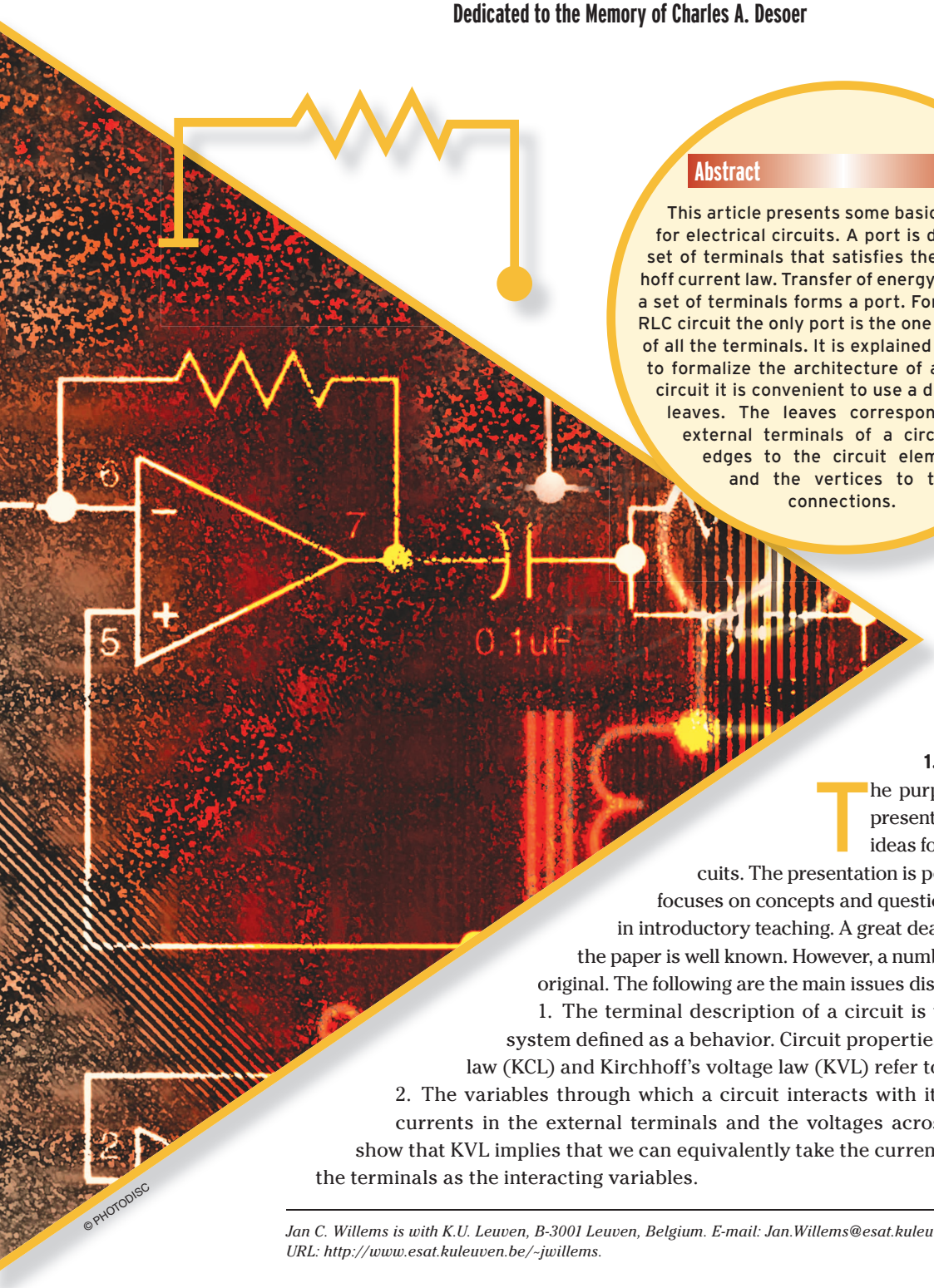
Terminals and Ports

Dedicated to the Memory of Charles A. Desoer



Abstract

This article presents some basic concepts for electrical circuits. A port is defined as a set of terminals that satisfies the port-Kirchhoff current law. Transfer of energy occurs when a set of terminals forms a port. For a connected RLC circuit the only port is the one that consists of all the terminals. It is explained that in order to formalize the architecture of an electrical circuit it is convenient to use a digraph with leaves. The leaves correspond to the external terminals of a circuit, the edges to the circuit elements, and the vertices to the connections.

Jan C. Willems

1. Introduction

The purpose of this article is to present a number of elementary ideas for modeling electrical circuits. The presentation is pedagogical in nature and focuses on concepts and questions that are of relevance in introductory teaching. A great deal of what is presented in the paper is well known. However, a number of ideas appear to be original. The following are the main issues discussed.

1. The terminal description of a circuit is viewed as a dynamical system defined as a behavior. Circuit properties as Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL) refer to the behavior.
2. The variables through which a circuit interacts with its environment are the currents in the external terminals and the voltages across these terminals. We show that KVL implies that we can equivalently take the currents and the potentials of the terminals as the interacting variables.

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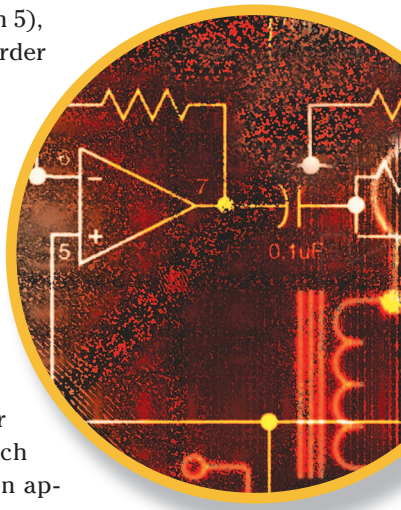
3. The central question addressed in the paper is when we can speak of the energy that is transferred from the environment to a circuit along a set of terminals. We argue that this requires that the sum of the currents on these terminals is zero. A set of terminals that satisfies this condition is called a port. The requirement that the sum of the currents in the terminals of a port is zero is called port-KCL.
4. Interconnection of circuits leads to conditions that state that the interconnected terminals share the current and the potential.
5. Interconnection is distinct from energy exchange. Terminals are for interconnection, ports are for energy transfer. Interconnection imposes *local* constraints on variables, while energy exchange is due to *action at a distance*, as it involves variables that happen at different locations in a physical system. In particular, for an interconnected circuit, it is in general not possible to speak about the energy that is transferred from one subcircuit to another, nor is it possible to speak about the energy that is transferred from the environment to a subcircuit.
6. It is common to deal with circuits in terms of digraphs. However, we argue that digraphs with leaves are a more convenient way to formalize a circuit architecture. Leaves are like edges that are incident with only one vertex. Digraphs with leaves give the external terminals a distinguished role, something that edges do not do. Also for hierarchical modeling and for incorporating circuit elements that do not consist of just 2-terminal ports (as 3-terminal elements), graphs with leaves appear to be the appropriate notion.
7. These ideas are applied to the modeling of RLC circuits. The models obtained contain in addition to the manifest variables the model aims at (the terminal currents and potentials), also auxiliary latent variables (for the modeling method presented, these are the edge currents and the vertex potentials). As usual when modeling physical systems new variables need to be introduced in addition to those whose behavior the model aims at.
8. We prove that for a connected RLC circuit the only port is the one that consists of all the terminals. In order to have non-trivial ports, a circuit needs to contain elements that are themselves multiports, as transformers.
9. We present a definition of passivity that states that a circuit is passive if at any time only a finite amount of energy can be extracted from it. Passivity is preserved by interconnection.
10. We prove that for passive linear time-invariant circuits port-KCL, a condition on the currents in the terminals of a port, is equivalent to port-KVL, a condition on the potentials of the terminals of a port.

The main contributions of this article are

i) the notion of a port (item 3) and its physical significance (item 5),
ii) digraphs with leaves in order to model circuits (item 6).



Both these contributions appear to be original. The paper is in a sense a sequel to [8] where many of the modeling issues discussed here for circuits have been developed for general dynamical systems. We believe that the ideas presented in this paper provide a systematic approach to the modeling of circuits, an approach that puts the physics central at all times. The material presented makes contact with numerous textbooks in electrical circuit theory. For a general introduction, see [2] and [1]. For graphs and electrical circuits, see [7]. The approach taken here, which uses the terminal behavior as the model of a circuit (see item 1) has roots in the work of McMillan [4] and Newcomb [5].

2. Currents and Voltages

We view an electrical circuit as a device, a black-box, with wires, called terminals, through which the circuit can interact electrically with its environment (see Figure 1). Circuit modeling often aims at describing this interaction. In the present section, we formulate this problem mathematically.

The first question that emerges is to specify the variables through which this interaction takes place. The most natural choice is to take as the relevant variables the currents that flow in the circuit terminals and the voltages across each pair of terminals (see Figure 2).

For ease of exposition, we standardize the positive direction of current flow. We assume that the current is counted as > 0 when it flows into the circuit. This direction is indicated by putting an arrow next to each terminal. V_{k_1,k_2} is the voltage drop from terminal k_1 to terminal k_2. The I_k's and the V_{k_1,k_2}'s are in principle measurable with ammeters and voltmeters.

Organize the currents as an N-dimensional vector and the voltages as an $N \times N$-dimensional matrix

KVL is evident and leads to potentials, while KCL imposes a genuine restriction on a circuit.

$$I = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix}, \quad V = \begin{bmatrix} V_{1,1} & V_{1,2} & \cdots & V_{1,N} \\ V_{2,1} & V_{2,2} & \cdots & V_{2,N} \\ \vdots & \vdots & \vdots & \vdots \\ V_{N,1} & V_{N,2} & \cdots & V_{N,N} \end{bmatrix}.$$

The circuit laws lead to a dynamical system (in the sense explained in Sidebar 1) $\Sigma_{IV} = (\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^{N\times N}, \mathcal{B}_{IV})$. For a circuit it is natural to take $\mathbb{R}$ for the time set. The signal space is the Cartesian product of $\mathbb{R}^N$, for the vector of currents, and $\mathbb{R}^{N\times N}$, for the matrix of voltages. $(I, V) \in \mathcal{B}_{IV}$ means that the time-trajectory

$$(I_1, I_2, \ldots, I_k, \ldots, I_N, V_{1,1}, V_{1,2}, \ldots, V_{k_1,k_2}, \ldots, V_{N,N}) : \mathbb{R} \to \mathbb{R}^N \times \mathbb{R}^{N\times N}$$

is compatible with the circuit architecture and its element values.

$(I, V) \in \mathcal{B}_{IV}$ means that whatever environment the circuit operates in, whatever termination is applied to it, or whatever larger circuit it is embedded in, the current voltage trajectory (I, V) will obey the laws imposed by $\mathcal{B}_{IV}$. The drawing of Figure 2 certainly does not suggest that the circuit terminals are open circuits. Nor is it meant to suggest that current or voltage sources should be applied at the external terminals. One should think of $\mathcal{B}_{IV}$ in the way one thinks of Ohm's law: whatever happens at the terminals, the current in the terminals and the voltage across the terminals of an Ohmic resistor obey Ohm's law.

We assume that the circuits which we consider obey *Kirchhoff's current law* (KCL) and *Kirchhoff's voltage law* (KVL). KCL states that

$$[\![(I, V) \in \mathcal{B}_{IV}]\!] \Rightarrow [\![I_1 + I_2 + \cdots + I_N = 0]\!]. \quad \text{(KCL)}$$

KVL states that

$$[\![(I, V) \in \mathcal{B}_{IV} \text{ and } k_1, k_2, \ldots, k_n \in \{1, 2, \ldots, N\}]\!] \Rightarrow [\![V_{k_1,k_2} + V_{k_2,k_3} + V_{k_3,k_4} + \cdots + V_{k_{n-1},k_n} + V_{k_n,k_1} = 0]\!]. \quad \text{(KVL)}$$

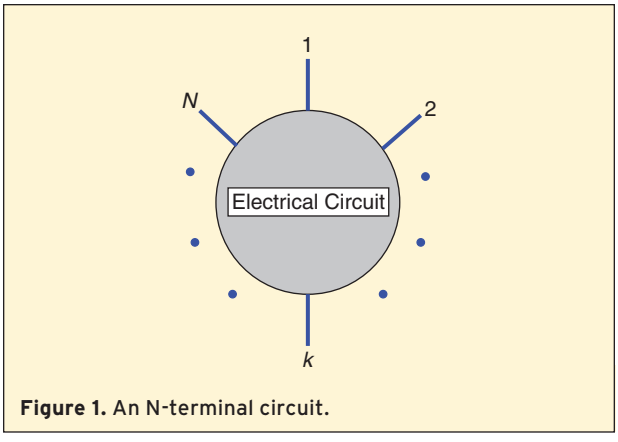


Figure 1. An N-terminal circuit.

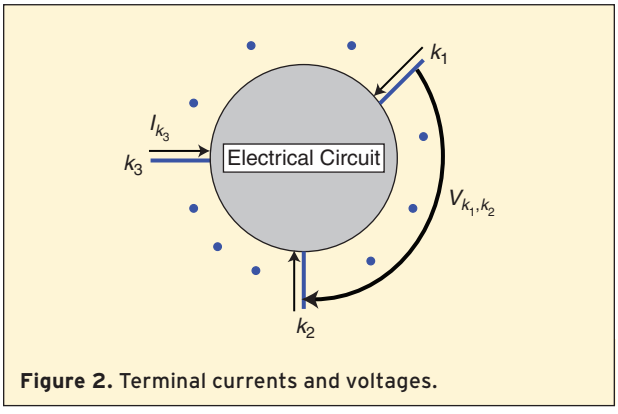


Figure 2. Terminal currents and voltages.

For $n = 2$ and $n = 3$, KVL leads to

$$V_{k_1,k_2} = -V_{k_2,k_1} \text{ and } V_{k_1,k_2} + V_{k_2,k_3} + V_{k_3,k_1} = 0.$$

It is easy to see that KVL holds if and only if it holds for $n = 3$. We view KVL as a universal law resulting from the physical nature of voltage drops. KCL means that the total current that flows into the circuit along all the terminals is zero, equivalently, that the circuit stores no net electrical charge. It imposes a constraint on the circuits considered.

3. Voltages and Potentials

KVL implies that instead of using the voltages across the terminals, we may equivalently use potentials. In this section, we explain the nature of this equivalence.

Theorem: *$V : \mathbb{R} \to \mathbb{R}^{N\times N}$ satisfies KVL if and only if there exists $P : \mathbb{R} \to \mathbb{R}^N$ such that $V_{k_1,k_2} = P_{k_1} - P_{k_2}$ for all $k_1, k_2 \in \{1, 2, \ldots, N\}$. P is called a* potential vector. *Let $e \in \mathbb{R}^N$ denote $e := [1 \quad 1 \quad \cdots \quad 1]^\top$. If P is a potential vector associated with V, then so is $P + \alpha e$ for all $\alpha : \mathbb{R} \to \mathbb{R}$.*

In order to prove this theorem, observe that the 'if'-part is obvious. For the 'only if'-part, choose $P_k = V_{k,1}$. KVL implies $V_{k_1,k_2} + V_{k_2,1} + V_{1,k_1} = 0$. Since, by KVL, $V_{k_1,1} + V_{1,k_1} = 0$, we obtain $V_{k_1,k_2} = -V_{1,k_1} - V_{k_2,1} = V_{k_1,1} - V_{k_2,1}$. Hence $V_{k_1,k_2} = P_{k_1} - P_{k_2}$, as claimed. The fact that one can add α to all the components of P is clear.

DYNAMICAL SYSTEMS

In this sidebar we explain the formalization of a dynamical system as a behavior. This point of view has been developed extensively in the last two decades (see [8] and its references). In the context of circuit theory, this definition is completely in the spirit of what is put forward in the work of McMillan [4] and Newcomb [5]. One of the main ideas of the behavioral approach is that it allows to avoid thinking of (open) dynamical systems in terms of inputs and outputs, to avoid thinking of the architecture of an interconnected systems in terms of signal flow graphs connecting subsystems, and to avoid thinking of interconnection as assigning the output to one subsystem to be the input of another subsystem. The motivation is that a physical system, for example an electrical circuit, is not a a signal processor, and that the dynamical laws that govern physical systems merely impose restrictions on the system variables, and do not express a cause/effect relation. Imposing a compatibility relation on the variables involved, without expressing what causes what, is what the gas law does, it is what the equations of circuit elements do, it is what Newton's second law does, it is what Maxwell's equations do.

A dynamical system is formally defined as a triple $\Sigma = (\mathbb{T}, \mathbb{W}, \mathscr{B})$, with $\mathbb{T} \subseteq \mathbb{R}$ the *time set*, $\mathbb{W}$ the *signal space*, and $\mathscr{B} \subseteq \mathbb{W}^{\mathbb{T}}$ the *behavior*. The time set expresses over which time instances the system evolves. Often, as for circuits, $\mathbb{T}$ is taken to be all of $\mathbb{R}$. The signal space expresses in which set the variables whose time evolution is modeled take on their values. Often, as in lumped circuits, $\mathbb{W}$ is a finite dimensional real vector space, while for distributed circuits, $\mathbb{W}$ is an infinite dimensional space, and for discrete event systems, $\mathbb{W}$ is a finite set. As the notation $\mathscr{B} \subseteq \mathbb{W}^{\mathbb{T}}$ indicates ($\mathbb{W}^{\mathbb{T}}$ denotes the set of maps from $\mathbb{T}$ into $\mathbb{W}$), the behavior is a set of time functions $w: \mathbb{T} \to \mathbb{W}$; $w \in \mathscr{B}$ means that the trajectory w is compatible with the laws of the system, while $w \notin \mathscr{B}$ means that the laws of the system forbid w to happen. Usually, the behavior $\mathscr{B}$ is described by behavioral equations, often differential equations.

System properties are conveniently defined in terms of the behavior. $\Sigma = (\mathbb{T}, \mathbb{W}, \mathscr{B})$ is said to be *linear if* $\mathbb{W}$ is a vector space and $\mathscr{B}$ is a linear subspace of $\mathbb{W}^{\mathbb{T}}$. Σ is said to be *time-invariant* if $\mathbb{T} = \mathbb{R}$, $[0, \infty)$, $\mathbb{Z}$, or $\mathbb{Z}_+$ and if $\sigma^t\mathscr{B} \subseteq \mathscr{B}$ for all $t \in \mathbb{T}$. Here σ^t denotes the t-shift, defined by $\sigma^T(f)(t') := f(t' + t)$. An especially important class of dynamical systems are the linear time-invariant differential systems (see Sidebar 2).

The behavioral approach allows to deal with systems described by PDE's in roughly the same setting. In that case the set of independent variables, $\mathbb{T}$, is (a subset of) $\mathbb{R}^n$ ($n = 4$ for PDE's over time and space), $\mathbb{W}$, the set of dependent variables, is again the signal space, and $\mathscr{B} \subseteq \mathbb{W}^{\mathbb{T}}$ consists for of the set of solutions of a system of PDE's (see [8] for pointers to the relevant literature). For Maxwell's equations, $\mathbb{T} = \mathbb{R}^4$, $\mathbb{W} = \mathbb{R}^{10}$, and $\mathscr{B}$ consists of the solutions of Maxwell's PDE's.

KCL and KVL are often expressed by taking one of the terminals as the 'datum', and reducing the number of terminals to $N - 1$, by setting the potential of the datum terminal equal to zero and its current equal to minus the sum of the currents of the other terminals. However, we choose not to do that, since this assumption becomes cumbersome when considering interconnections in which the datum terminals may not be connected.

KVL allows to assume that the interaction of a circuit with its environment takes place through two real variables, a *current* and a *potential*, on each terminal (see Figure 3). The circuit laws lead to a dynamical system $\Sigma = (\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^N, \mathscr{B}_{\text{IP}})$. The signal space is the Cartesian product of $\mathbb{R}^N$, for the vector of currents, and $\mathbb{R}^N$,

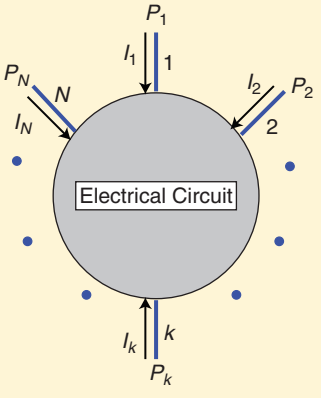


Figure 3. Terminal currents and potentials.

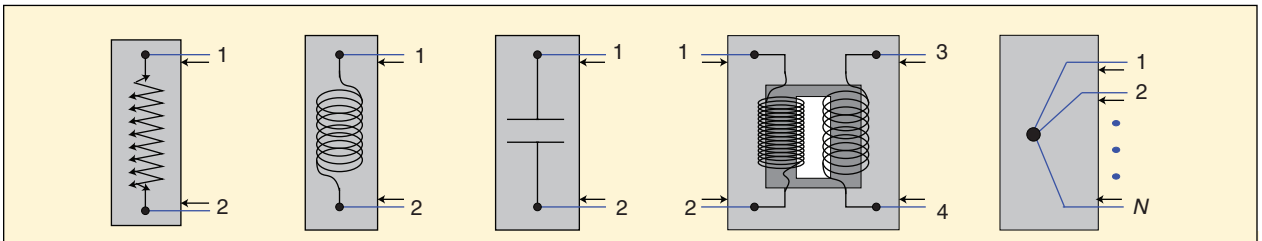


Figure 4. Circuit elements.

for the vector of potentials. Hence $(I, P) \in \mathcal{B}_{\text{IP}}$ means that the time-trajectory

$$(I_1, I_2, \ldots, I_N, P_1, P_2, \ldots, P_N) : \mathbb{R} \to \mathbb{R}^N \times \mathbb{R}^N$$

is compatible with the circuit architecture and its element values. Later in the paper we shall explain how $\mathcal{B}_{\text{IP}}$ can be obtained for RLC circuits. In terms of the current/potential behavior $\mathcal{B}_{\text{IP}}$, KCL becomes

$$[\![(I, P) \in \mathcal{B}_{\text{IP}}]\!] \Rightarrow [\![I_1 + I_2 + \cdots + I_N = 0]\!], \qquad \text{(KCL)}$$

while KVL states

$$[\![(I, P) \in \mathcal{B}_{\text{IP}} \text{ and } \alpha : \mathbb{R} \to \mathbb{R}]\!] \Rightarrow [\![(I_1, I_2, \ldots, I_N, P_1 + \alpha, P_2 + \alpha, \ldots, P_N + \alpha) \in \mathcal{B}_{\text{IP}}]\!]. \qquad \text{(KVL)}$$

Examples: The behavior of the classical circuit elements (see Figure 4) are defined as the set of solutions of differential equations (we consider algebraic equations as differential equations of order 0).

Resistors, inductors, and capacitors are 2-terminal circuits with behavioral equations

$$\begin{aligned} \text{resistor:} \quad & P_1 - P_2 = R\, I_1, \quad I_1 + I_2 = 0, \\ \text{inductor:} \quad & P_1 - P_2 = L \frac{d}{dt} I_1, \quad I_1 + I_2 = 0, \\ \text{capacitor:} \quad & C \frac{d}{dt}(P_1 - P_2) = I_1, \quad I_1 + I_2 = 0, \end{aligned}$$

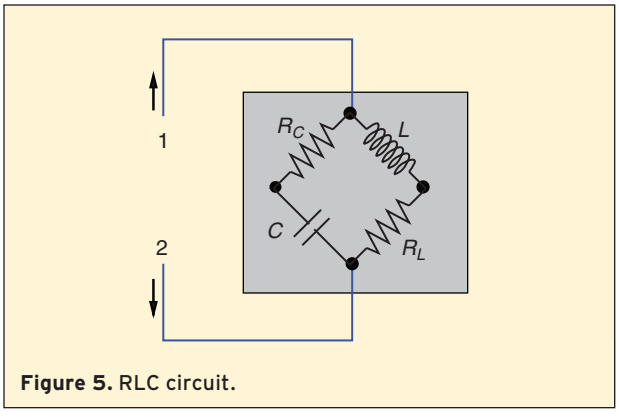


Figure 5. RLC circuit.

with R the resistance, L the inductance, and C the capacitance. Transformers have 4 terminals and behavioral equations

$$\text{transformer: } P_3 - P_4 = n\,(P_1 - P_2), \quad I_1 = -\,n\, I_3, I_1 + I_2 = 0,\ I_3 + I_4 = 0,$$

with n the transformer ratio. Other common circuit elements are voltage sources, current sources, open and short circuits, 4-terminal gyrators, 3-terminal transistors, and the connector, an N-terminal circuit with behavioral equations

$$\text{connector: } I_1 + I_2 + \cdots + I_N = 0, P_1 = P_2 = \cdots = P_N.$$

We give an example of a simple circuit composed of many elements, shown in Figure 5. Assume that $R_L, R_C, L, C > 0$. Deriving behavioral equations for this circuit, while straightforward, requires a bit of routine in elimination of variables from differential equations (see Sidebar 2). There are two cases to consider.

Case 1: $CR_C \neq L/R_L$. Then the behavioral equations are

$$\left(1 + (CR_C + L/R_L)\frac{d}{dt} + CR_C\, L/R_L \frac{d^2}{dt^2}\right) R_L\, I_1 = \left(1 + (1 + R_L/R_C) CR_C \frac{d}{dt} + L\, C \frac{d^2}{dt^2}\right)(P_1 - P_2), \quad I_1 + I_2 = 0.$$

Case 2: $CR_C = L/R_L$. Then the behavioral equations are

$$\left(1 + CR_C \frac{d}{dt}\right) R_L\, I_1 = \left(1 + CR_L \frac{d}{dt}\right)(P_1 - P_2),\ I_1 + I_2 = 0.$$

Note that the transition from case 1 to case 2 may be explained as a cancelation of a common factor from the differential operators on the left and the right hand sides of the differential equation for case 1. However, when $CR_C = L/R_L$ and $R_C = R_L$, then a second common factor appears, but this common factor cannot be canceled. This subtle issue of canceling common factors is related to controllability (see Sidebar 2). Controllability is discussed extensively in [8].

LINEAR DIFFERENTIAL SYSTEMS

A *linear time-invariant differential system* (LTIDS) is a dynamical system $\Sigma = (\mathbb{R}, \mathbb{R}^w, \mathscr{B})$ whose behavior $\mathscr{B}$ is the solution set of a system of ordinary differential equations (ODE's)

$$R\left(\frac{d}{dt}\right)w = 0, \quad \text{with } R \in R^{\bullet\times w}[\xi]. \qquad \text{(Ker)}$$

$R \in \mathbb{R}^{\bullet\times w}[\xi]$ means that R is a matrix of polynomials with real coefficients, with w rows and any finite number of columns. In order to define the corresponding behavior, we need to specify when we consider $w : \mathbb{R} \to \mathbb{R}^w$ to be a solution of (Ker). For ease of exposition, we think of infinite differentiable solutions. Other possibilities, as taking distributional solutions, or solutions in $\mathscr{L}^{\text{local}}(\mathbb{R}, \mathbb{R}^w)$, and with the ODE's in (Ker) interpreted in the sense of distributions, have something to be said for.

The behavior defined by (Ker) is

$$\mathscr{B} = \{w \in \mathscr{C}^\infty(\mathbb{R}, \mathbb{R}^w) \mid R\left(\frac{d}{dt}\right)w(t) = 0 \text{ for all } t \in \mathbb{R}\}$$

Obviously, $\mathscr{B} = \text{kernel}\,(R(d/dt))$, with $(R(d/dt))$, viewed as a differential operator mapping $\mathscr{C}^\infty(\mathbb{R}, \mathbb{R}^w)$ to $\mathscr{C}^\infty(\mathbb{R}, \mathbb{R}^\bullet)$. We call (Ker) a *kernel representation* of the corresponding dynamical system. There are many other useful representations of the same behavior.

Much is known about LTIDSs. We explain four central results concerning LTIDSs.

Uniqueness of kernel representations: A kernel representation of a given LTIDS is far from unique, but using the language of modules, it is possible to classify the non-uniqueness of this representation. There is a one-to-one relation between the set of LTIDSs with w variables and the $\mathbb{R}[\xi]$-submodules of $\mathbb{R}^w[\xi]$. This one-to-one relation associates with kernel $(R(d/dt))$ the $\mathbb{R}[\xi]$-module generated by the rows of R. This result implies that each LTIDS allows a representation (Ker) with R of full row rank, called a *minimal* kernel representation. Two minimal kernel representations $R_1(d/dt)w = 0$ and $R_2(d/dt)w = 0$ define the same behavior if and only if there exists a unimodular real polynomial matrix U such that $R_1 = UR_2$.

Elimination of latent variables: *Every image is a kernel.* More precisely, for each $M \in \mathbb{R}^{\bullet\times w}[\xi]$, there exists $R \in \mathbb{R}^{w\times\bullet}[\xi]$ such that

$$\text{kernel}\,(R(d/dt)) = \text{image}\,(M(d/dt)).$$

This result immediately implies the *elimination theorem.* This theorem states the following. Consider the system of ODE's

$$R(d/dt)w = M(d/dt)\ell$$

linking the signals $w : \mathbb{R} \to \mathbb{R}^w$ and $\ell : \mathbb{R} \to \mathbb{R}^\ell$, through the above ODE with $R \in \mathbb{R}^{\bullet\times w}[\xi]$ and $M \in \mathbb{R}^{\bullet\times\ell}[\xi]$. Assume that we are only interested in the behavior of the signals w, but that the equations governing w involve also the auxiliary variables ℓ. We call the w's *manifest* variables, and the ℓ's *latent* variables. The resulting behavior w-behavior is

$$\mathscr{B} = \{w \in \mathscr{C}^\infty(\mathbb{R}, \mathbb{R}^w) \mid \text{there exists } \ell \in \mathscr{C}^\infty(\mathbb{R}, \mathbb{R}^\ell) \text{ such that } R(d/dt)w = M(d/dt)\ell\}$$

The elimination theorem says that $\mathscr{B}$ is a LTIDS. In other words, there exists $R' \in \mathbb{R}^{w\times\bullet}[\xi]$ such that

$$\mathscr{B} = \text{kernel}\left(R'\left(\frac{d}{dt}\right)\right).$$

Note that in the resulting equations $R'(d/dt)w = 0$ for the variables w, the auxiliary variables ℓ have been completely eliminated. There exist effective algorithms for passing from (R, M) to R'.

The situation where latent variables are introduced in modeling is very common, for example, when modeling interconnected systems, as electrical circuits, with the w's the variables on the external terminals, and the ℓ's internal variables on the interconnected terminals of the circuit elements. In Sections 8 and 10, we have seen how the modeling of interconnected systems in general, and RLC circuits in particular leads to the introduction of auxiliary variables. Another example where auxiliary variables occur are state equations, with the states viewed as auxiliary variables. Note that the elimination theorem implies that the external current/voltage behavior of a linear RLC circuit is a system of constant coefficient linear differential equations, since the equations (CE), which involve also latent variables, are constant coefficient differential equations. ■

Controllability and image representations: *A kernel is an image if and only if the corresponding behavior is controllable.*

A LTIDS with behavior $\mathscr{B}$ is said to be *controllable* if for all $w_1, w_2 \in \mathscr{B}$, there exists a $T \geq 0$ and a $w \in \mathscr{B}$ such that

$$w(t) = \begin{cases} w_1(t) & \text{for } t \leq 0, \\ w_2(t-T) & \text{for } t > T. \end{cases}$$

In other words, a system is controllable if every two trajectories can be concatenated after a delay. The main virtue of this definition is that it makes controllability into a genuine system property, rather than merely a property of a state space representation, as is the case for the usual definition of (state) controllability.

The system governed by (Ker) with behavior $\mathscr{B}$ is controllable if and only if there exists a $M \in \mathbb{R}^{\bullet \times w}[\xi]$ such that

$$\mathscr{B} = \text{image}\left(M\left(\frac{d}{dt}\right)\right).$$

In other words, controllability holds if and only if the w-behavior can be described in terms of latent variables ℓ by

$$w = M\left(\frac{d}{dt}\right)\ell, \text{ with } M \in \mathbb{R}^{w \times \bullet}[\xi]. \qquad \text{(Im)}$$

(Im) is called an *image representation* of the resulting w-behavior. The relation between image representations and controllability leads to effective tests for verifying controllability.

Another necessary and sufficient condition for controllability of the system defined by (Ker) is

$$[\![(\text{Ker}) \text{defines a controllable system}]\!] \Leftrightarrow [\![\text{the rank of } R(\lambda) \in \mathbb{C}^{\bullet \times w} \text{ is the same for all } \lambda \in \mathbb{C}]\!].$$

See [8] for a further discussion of conditions for controllability and the relation with state controllability. ■

Existence of a componentwise input/output partition: Let $\mathscr{B}$ be the behavior of a LTIDS. By permuting the components of w, $w = \begin{bmatrix} u \\ y \end{bmatrix}$, we obtain the minimal kernel representation

$$P\left(\frac{d}{dt}\right)y = Q\left(\frac{d}{dt}\right)u$$

for $\mathscr{B}$, with P, Q real polynomial matrices, P square, and $\texttt{determinant}\ (P) \neq 0$. This implies that $\mathscr{B}$ leaves u free, and that y is generated by u and the initial conditions. In system theory parlance, u is input, and y is output. The matrix of rational functions $P^{-1}Q$ is called the *transfer function* of the input/output system. The transfer function specifies the corresponding behavior uniquely if and only the system is controllable. In general, the transfer function specifies only the controllable part of a system. In particular, for linear time-invariant circuits, the impedance or the admittance determine only the controllable part of the behavior. Non-degenerate physical systems can become uncontrollable. For example, the terminal behavior of the circuit of Figure 5 becomes uncontrollable when $CR_C = L/R_L$ and $R_C = R_L$. ■

The above results hold, *mutatis mutandis*, for discrete time systems. This generalization is straightforward. The results about modules, elimination, and controllability and image representations also hold for systems described by constant coefficient PDE's [6]. For example, Maxwell's equations define a controllable system. The generalization to PDE's is mathematically deep and relevant for unifying the theory of systems described by ODE's and PDE's.

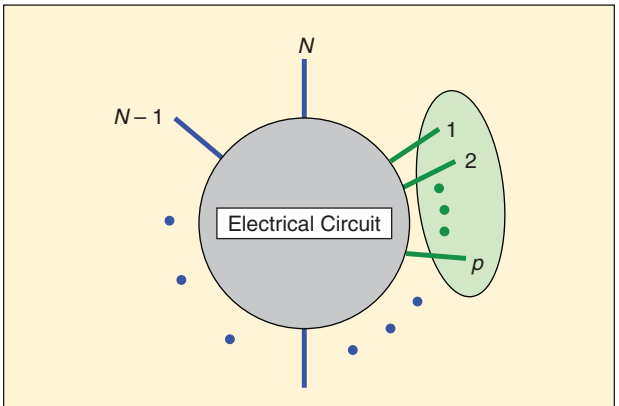


Figure 6. Port.

4. Ports

Under what conditions can we speak about the electrical power and of the energy that flows in or out of the circuit along a set of terminals of a circuit?

This is the main issue discussed in this paper.

Consider an N-terminal circuit with current/potential behavior $\mathscr{B}_{\text{IP}}$. Single out p terminals. Assume that these are the first p terminals (see Figure 6).

$$\Big[\!\Big[\text{Terminals } \{1, 2, \ldots, p\} \text{ are said to form a } \textit{port}\Big]\!\Big] : \Leftrightarrow$$
$$\Big[\!\Big[[\![(I_1, I_2, \ldots, I_p, I_{p+1}, I_{p+2}, \ldots, I_N, P_1, P_2, \ldots, P_p, P_{p+1}, P_{p+2}, \ldots, P_N) \in \mathscr{B}_{\text{IP}}]\!] \Rightarrow [\![I_1 + I_2 + \cdots + I_p = 0]\!]\Big]\!\Big]. \quad \text{(port-KCL)}$$

We call this property the *port-Kirchhoff current law* (port-KCL).

If the terminals $\{1, 2, \ldots, p\}$ form a port, then the power delivered to the circuit at time t along these terminals is equal to

$$\text{power} = I_1(t)P_1(t) + I_2(t)P_2(t) + \cdots + I_p(t)P_p(t)$$

and the energy delivered during the time-interval $[t_1, t_2]$ is equal to

$$\text{energy} = \int_{t_1}^{t_2} [I_1(t)P_1(t) + I_2(t)P_2(t) + \cdots + I_p(t)P_p(t)]\, dt.$$

We emphasize that this physical interpretation in terms of power and energy is valid only if the terminals form a port. If port-KCL is not satisfied, then this expressions have the dimension of power and energy, but they need not be physical power and energy. We discuss the physical justification of these expressions in Section 13.

Note that KCL implies that the complete set of terminals forms a port. It follows that the terminals of R's, L's, and C's form a port. For a transformer, terminals $\{1, 2\}$ and $\{3, 4\}$, and, of course, $\{1, 2, 3, 4\}$ form ports. In Section 9 we will prove that a connected linear RLC circuit only has one port, namely the port consisting of all the terminals. In order for sub-ports to exist, we need disconnected circuits, or circuits with multi-port elements like transformers or gyrators.

It is easy to prove that a pair of terminals that is terminated with a transformer (for example $\{1, 2\}$ in Figure 7) forms a port. However, adding a unit transformer in general changes the circuit behavior. For example, it sets the current into the third terminal of a 3-terminal circuit that satisfies KCL to zero.

For the circuit shown in Figure 8, terminals $\{1, 2, 3, 4\}$ form a port. But $\{1, 2\}$ and $\{3, 4\}$ do not. It is therefore not possible to speak about the energy that is transferred from terminals $\{1, 2\}$ to terminals $\{3, 4\}$. However, adding unit transformers (see Figure 9) turns $\{1, 2\}$ and $\{3, 4\}$ into ports.

Consider a 2-terminal circuit. If KCL is satisfied, then $I_1 + I_2 = 0$, while KVL implies that the circuit behavior involves only the potential difference $P_1 - P_2$. In this case, one may as well take as the circuit variables the current $I = I_1 = -I_2$ and the voltage $V = P_1 - P_2$, as shown in Figure 10.

The circuit terminals form a port, and the power that flows into the circuit along the port equals $I_1P_1 + I_2P_2 = IV$. The notion of a port involving 2 terminals is standard in the literature. In view of the fact that sub-ports are exceptional, unless the circuit includes elements like transformers, it is more difficult to appreciate the origin of the interest in N-ports (see Section 6).

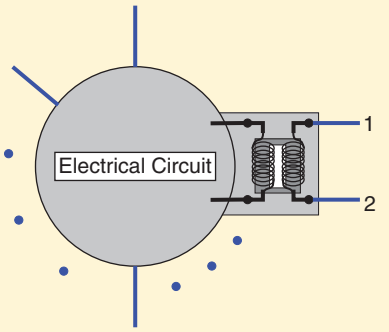


Figure 7. Termination with a unit transformer.

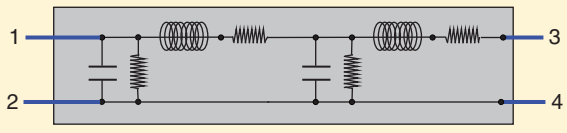


Figure 8. A transmission line.

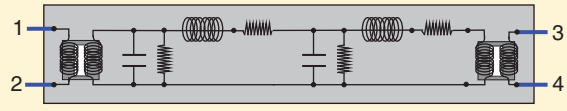


Figure 9. A transmission line terminated by unit transformers.

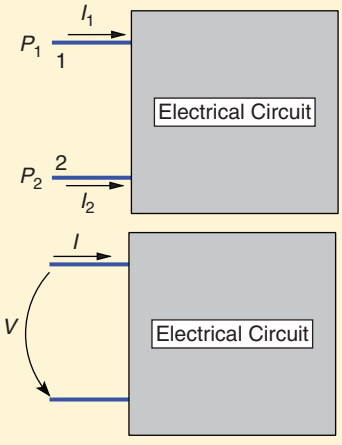


Figure 10. A 2-terminal 1-port.

5. Internal Ports

Until now, we have considered the behavior of the variables on the external terminals through which a circuit interacts with its environment. In many circumstances, a model of a circuit is needed that describes not only the

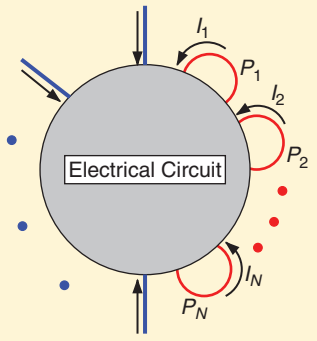


Figure 11. A circuit with internal terminals.

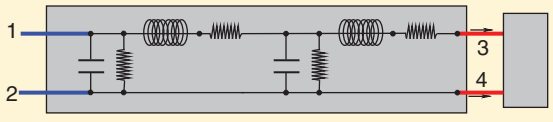


Figure 12. A transmission line with a termination.

behavior of the variables on the external terminals, but the behavior of certain variables inside the circuit, or a combination of internal and external variables. These internal variables could in principle be any combination or function of internal and external currents and potentials. However, since we are interested in discussing energy flow, we will be concerned with the currents and the potentials (assuming KVL) on certain of the internal terminals, as shown in Figure 11.

Assume that there are N internal terminals, denoted $\{1, 2, \ldots, N\}$. In the case of external terminals, we were able to standardize the direction of positive current flow by assuming that the current is > 0 when it flows into the circuit. This convention is not possible for internal terminals. We are therefore assuming that the internal terminals are given a direction, indicated by an arrow, and that the current is > 0 when it flows in the direction of the arrow (see Figure 11). Assuming KVL, the circuit laws lead to a dynamical system $\Sigma = (\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^N, \mathscr{B}_{\text{IP}})$, where $(I, P) \in \mathscr{B}_{\text{IP}}$ means that the time-function

$$(I, P) = (I_1, I_2, \ldots, I_N, P_1, P_2, \ldots, P_N) : \mathbb{R} \to \mathbb{R}^N \times \mathbb{R}^N$$

is compatible with the architecture of the circuit and the values of the elements in the circuit.

$$\Big[\!\Big[\text{Terminals } \{1, 2, \ldots, N\} \text{ are said to form an } \textit{internal port}\Big]\!\Big]:$$
$$\Leftrightarrow \Big[\!\Big[[\![(I_1, I_2, \ldots, I_N, P_1, P_2, \ldots, P_N) \in \mathscr{B}_{\text{IP}}]\!]$$
$$\Rightarrow [\![\, I_1 + I_2 + \cdots + I_N = 0]\!] \Big]\!\Big]. \qquad \text{(port-KCL')}$$

We call this property the *internal port-Kirchhoff current law*. If the terminals $\{1, 2, \ldots, N\}$ form an internal port, then the power that flows through the terminals from one side of the circuit to the other side in the direction indicated by the arrows is equal to

$$\text{power} = I_1(t)P_1(t) + I_2(t)P_2(t) + \cdots + I_N(t)P_N(t)$$

and the energy is equal to

$$\text{energy} = \int_{t_1}^{t_2} [I_1(t)P_1(t) + I_2(t)P_2(t) + \cdots + I_N(t)P_N(t)]\, dt.$$

We emphasize that this physical interpretation in terms of power and energy is valid only if the terminals form an internal port.

In the same vein as for external and internal ports, we can consider mixed ports, involving both external and internal terminals.

As an example of an internal port, consider the circuit shown in Figure 12. Assuming that the subcircuit on the right is a 2-terminal 1-port (think of it as a load), then terminals $\{3, 4\}$ form an internal port, and so we can speak of the energy transferred from the circuit to the load. Terminals $\{1, 2\}$ in turn now form an external 2-terminal 1-port, so for the case at hand it is possible to speak about the energy transferred from the external port to the load. Of course, this is not a consequence of the laws of the circuit shown in Figure 8, but a consequence of the termination at terminals $\{3, 4\}$. When terminals $\{1, 2\}$ are also terminated by a 2-terminal 1-port (think of it as a source), then both $\{1, 2\}$ and $\{3, 4\}$ form internal ports, and it is possible to speak about the energy that is transferred by the transmission line from the source to the load.

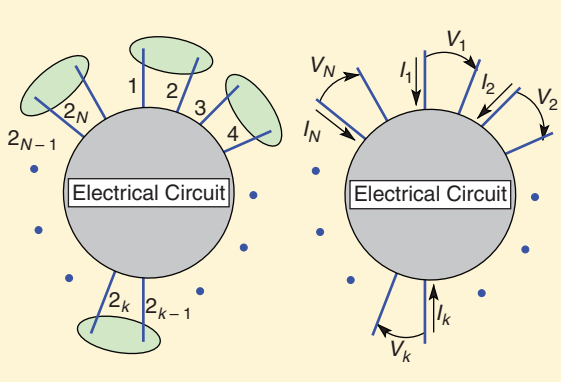


Figure 13. N-port.

6. *N*-Ports

As explained in Section 4, a 2-terminal circuit that satisfies KVL is a 1-port. There is no reason, of course, why a 4-terminal circuit should be a 2-port consisting of two 2-terminal 1-ports. However, studying a 4-terminal circuit as if it were a 2-port can be very useful in view of the intended use of the circuit, for example, as a device that transfers energy from a source to a load, in the spirit of the remarks made at the end of the previous section for the circuits of Figures 8 and 12. The generalization of this idea to general circuits with an even number of terminals leads to N-ports. We discuss these in the present section.

Consider an $2N$-terminal circuit. Denote its current/potential behavior by $\mathscr{B}_{\text{IP}} \subseteq (\mathbb{R}^{2N} \times \mathbb{R}^{2N})^{\mathbb{R}}$. Assume that the terminals are paired into $\{1, 2\}, \{3, 4\}, \ldots, \{2N-1, 2N\}$, as shown in Figure 13. Now *impose* the following relations on the terminal variables:

$$I_1 + I_2 = 0,\ I_3 + I_4 = 0, \ldots,$$
$$I_{2k-1} + I_{2k} = 0, \ldots, I_{2N-1} + I_{2N} = 0.$$

Define as new variables the currents into terminals $1, 3, \ldots, 2N-1$ and the voltages across the terminal pairs $\{1, 2\}, \{3, 4\}, \{2N-1, 2N\}$. This leads to the *port behavior* defined by

$$\mathscr{B}_{\text{port}} := (I_1, I_2, \ldots, I_N, V_1, V_2, \ldots, V_N) : \mathbb{R} \to \mathbb{R}^{2N} \times \mathbb{R}^{2N} \mid$$
$$\exists\, P_1, P_3, \ldots, P_{2N-1} : \mathbb{R} \to \mathbb{R} \text{ such that}$$
$$(I_1, -I_1, I_2, -I_2, \ldots, I_N, -I_N, P_1, P_1 - V_1, P_3, P_3 - V_2, \ldots,$$
$$P_{2N-1}, P_{2N-1} - V_N) \in \mathscr{B}_{\text{IP}}.$$

The power entering a circuit that operates in a port behavior mode at the port $\{2k-1, 2k\}$ equals $I_k V_k$. The total power is obtained by adding the power port-by-port. We can also return to the original circuit of Figure 6 and *impose* on the behavior $\mathscr{B}_{\text{IP}}$ the condition $I_1 + I_2 + \cdots + I_p = 0$, and then discuss, for the subbehavior obtained with this constraint added, power and energy flow at the terminals $\{1, 2, \ldots, p\}$.

The port behavior of a circuit is not part of the physics of a circuit, but rather a consequence of the intended use of the circuit. For 2-terminal circuits, the port behavior is all what matters. Viewing a 4-terminal circuit as a 2-port consisting of two 2-terminal 1-ports has a clear motivation in terms of studying energy transfer from a source to a load. But it is more difficult to appreciate the classical interest in N-ports, except in the context of reactance or resistor extraction. However, as a general idea for studying multi-terminal circuits, N-ports appear ill-motivated. For example, the port behavior has undesirable consequences when applied to 3-terminal circuits, since assuming that two of the terminals act as a port forces the current in the third terminal to be zero.

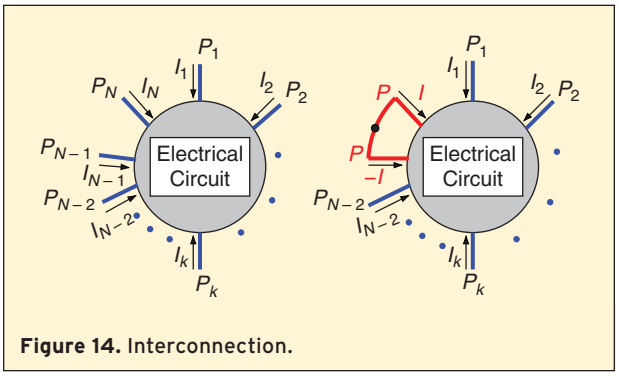


Figure 14. Interconnection.

Note that the port behavior as defined here is exactly what is obtained by terminating the terminal pairs $\{1, 2\}, \{3, 4\}, \ldots, \{2N-1, 2N\}$ with unit transformers. However, such unit transformers are rarely part of the physics of a circuit.

7. Interconnection

We view interconnection of circuits as connecting terminals, like soldering wires together. Assume that we have a circuit with N terminals that satisfies KVL. Connecting terminals $N-1$ and N, as shown in Figure 14, leads to imposing the relations

$$I_{N-1} + I_N = 0, \quad P_{N-1} = P_N.$$

This implies that after interconnection the terminals share the variables P_{N-1}, P_N, and I_{N-1}, I_N (up to a sign). Interconnection is therefore *variable sharing*. The interconnected circuit has $N-2$ external terminals. Its behavior is

$$\{(I_1, I_2, \ldots, I_{N-2}, P_1, P_2, \ldots, P_{N-2}) : \mathbb{R} \to \mathbb{R}^{N-2} \times \mathbb{R}^{N-2} \mid$$
$$\text{there exist } I, P \text{ such that } (I_1, I_2, \ldots,$$
$$I_{N-2}, I, -I, P_1, P_2, \ldots, P_{N-2}, P, P) \in \mathscr{B}_{\text{IP}}\}.$$

The connection of two terminals of two different circuits follows from the connection of two terminals of the same circuit. Assume that we have a circuit with N terminals, denoted $1, 2, \ldots, N$, and another with N' terminals, denoted $1', 2', \ldots, N'$. Connecting terminals N and N', as shown in Figure 15, leads to imposing the relations

$$I_N + I_{N'} = 0, \quad P_N = P_{N'}.$$

This implies that after interconnection circuit 1 and circuit 2 share the variables $P_N, P_{N'}$, and $I_N, I_{N'}$ (up to a sign).

The interconnected circuit has $N + N' - 2$ external terminals. Its behavior is

$$\{(I_1, \ldots, I_{N-1}, I_{1'}, \ldots, I_{N'-1}, P_1, \ldots, P_{N-1}, P_{1'}, \ldots, P_{N'-1}):$$

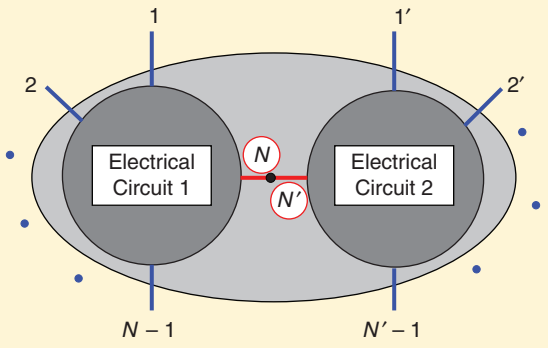


Figure 15. Interconnection of terminals of two circuits.

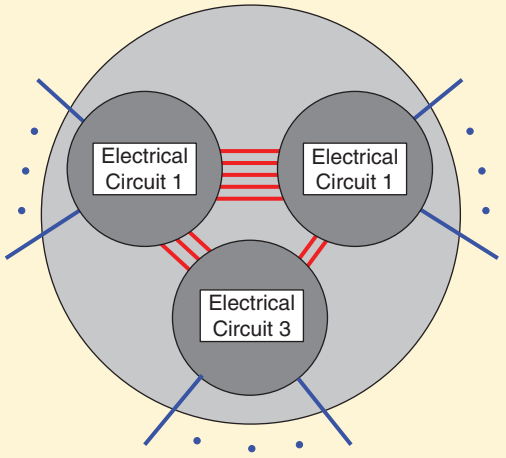


Figure 16. Interconnection of more terminals of more circuits.

$\mathbb{R} \to \mathbb{R}^{N+N'-2} \times \mathbb{R}^{N+N'-2} \mid$ there exist I, P such that $(I_1, \ldots, I_{N-1}, I, P_1, \ldots, P_{N-1}, P) \in \mathcal{B}_1$ and $(I_1, \ldots, I_{N'-1}, -I, P_1, \ldots, P_{N'-1}, P) \in \mathcal{B}_2\}$.

Once we have defined the interconnection of one pair of terminals, we obtain the interconnection of more terminals of more circuits as a straightforward generalization by connecting two terminals at the time (see Figure 16).

It is easy to see that interconnection preserves many circuit properties, in particular, KVL, KCL, linearity, time-invariance, reciprocity, and passivity. Passivity is discussed in Section 11. We do not discuss reciprocity further in the present article.

The following important conclusion can be drawn from our treatment of ports and terminals. The variables on the terminals of a circuit determine the interaction with the environment. Interconnection puts restrictions on the variables of particular terminals. Ports, on the other hand, involve sets of terminals.

DIGRAPHS WITH LEAVES

We assume that the reader is familiar with graphs and directed graphs, usually called digraphs. Digraphs play a central role in classical circuit theory. In Sections 9 and 10, we argue that for circuit applications (and for studying interconnected systems in general), it is convenient to introduce also edges that are incident with only one vertex. We call these special edges 'leaves'. In this sidebar, we give a formal definition of a digraph with leaves.

A *digraph with leaves* is defined as

$$(\mathbb{V}, \mathbb{E}, \mathbb{L}, f_{\mathbb{E}}, f_{\mathbb{L}})$$

with $\mathbb{V}$ a finite set of $|\mathbb{V}|$ *vertices*, $\mathbb{E}$ a finite set of $|\mathbb{E}|$ *edges*, $\mathbb{L}$ a finite set of $|\mathbb{L}|$ leaves, $f_{\mathbb{E}} : \mathbb{E} \to \mathbb{V}^2$, the *edge incidence map*, and $f_{\mathbb{L}} : \mathbb{L} \to \mathbb{V} \times \{\bullet\!\leftarrow, \bullet\!\rightarrow\}$ the *leaf incidence map*. If $f_{\mathbb{E}}(e) = (v_1, v_2)$, then we call e *incident* with v_1 and v_2; v_1 is called the *source* of e and v_2 is called the *sink* of e. We think of e as being directed from v_1 to v_2. If $f_{\mathbb{L}}(\ell) = v\bullet\!\leftarrow$ or $v\bullet\!\rightarrow$, then we call ℓ *incident* with v. If $f_{\mathbb{L}}(\ell) = v\bullet\!\rightarrow$, then v is called the *source* of ℓ and we think of ℓ as being directed away from v, while if $f_{\mathbb{L}}(\ell) = v\bullet\!\leftarrow$, then v is called the *sink* of ℓ and we think of ℓ as being directed towards v.

The edge e is called a *self-loop* if $f_{\mathbb{E}}(e) = (v, v)$.

A convenient way of specifying a digraph with leaves without self-loops is by its incidence matrices. The *edge incidence matrix* $\mathbb{A}_{\mathbb{E}}$ is a matrix with $|\mathbb{V}|$ rows and $|\mathbb{E}|$ columns. Its elements are 0, 1, or -1, with the (i,j)-th element equal to 1 if vertex v_i is the source for edge e_j, -1 if vertex v_i is the sink for edge e_j, and 0 if vertex v_i is not incident with edge e_j. The *leaf incidence matrix* $\mathbb{A}_{\mathbb{L}}$ is a matrix with $|\mathbb{V}|$ rows and $|\mathbb{L}|$ columns. Its elements are 0, 1, or -1, with the (i,j)-th element equal to 1 if vertex v_i is the source for leaf ℓ_j, -1 if vertex v_i is the sink for leaf ℓ_j, and 0 if vertex v_i is not incident with leaf e_j.

Digraphs with leaves having a moderate number of vertices, edges, and leaves can be represented pictorially in the obvious way. An example with 4 vertices, 5 edges, and 4 leaves is shown in Figure 17. The associated incidence matrices are given in Section 8.

Energy transfer happens via ports. Non-trivial ports always involve more than one terminal. It is not uncommon, as is done in bond graphs [3] or power based modeling, to think of system interconnection in terms of power exchange and conservation of energy. These ideas are unfortunately flawed. Even in simple situations as electrical circuits, energy transfer is not a *local* phenomenon but involves *action at a distance*.

Terminals are for interconnection, ports are for energy transfer

For example, for the interconnected circuit in Figure 16, is not possible to speak of *'the energy transferred from circuit 1 to circuit 2'*, or of *'the energy transferred from the environment to circuit 1'*, unless the relevant terminals form a port.

8. Modeling Circuits with 2-Terminal Ports

In this section, we deal with a classical problem: obtaining the terminal behavior of a linear RLC circuit. The most important point put forward is the following. For modeling circuits it is more convenient to use *digraphs with leaves* instead of simply digraphs, as is classically done. The reason is that we need to give the external terminals a special role. External terminals are connected to only one vertex, and this should be reflected in the associated graph. This leads to the leaves. The introduction of leaves may appear to be a somewhat minor point, but we believe that is pedagogically crucial. The notion of a digraph with leaves is discussed in Sidebar 3.

As an example, consider the circuit shown in Figure 17. The circuit has 4 external terminals, and it is not really possible to associate edges with these terminals. However, the introduction of leaves, as shown on the lower part of the figure, solves this dilemma.

We specify an RLC circuit as follows. The *circuit architecture* is a digraph with leaves without self-loops (we use the notation of Sidebar 3). Assume that all the leaves are directed into the vertex it is incident with (this corresponds with our convention that the currents in the external terminals are counted as >0 when they flow into the circuit). Denote the edge incidence matrix by $A_{\mathbb{E}}$ and the leaf incidence matrix by $A_{\mathbb{L}}$. The $|\mathbb{E}|$ edges correspond to the elements of the circuit (the R's, L's, and C's), the $|\mathbb{V}|$ vertices correspond to the connections, and the $|\mathbb{L}|$ leaves correspond to the external terminals. The specification of the elements in the edges is done by a map that associates with each edge either a resistance, an inductance, or a capacitance of a given value. This leads to three $|\mathbb{E}| \times |\mathbb{E}|$ diagonal real matrices $\mathscr{R}$, $\mathscr{L}$, and $\mathscr{C}$, defined as follows. The i-th diagonal element of $\mathscr{R}$, $\mathscr{L}$, and $\mathscr{C}$ equals respectively R_{e_i} if there is a resistor of value R_{e_i} in edge e_i, L_{e_i} if there is an inductor of value L_{e_i} in edge e_i, and C_{e_i} if there is a capacitor of value C_{e_i} in edge e_i, and 0 otherwise.

For the circuit in Figure 17 these parameter matrices are given by

$$\mathbb{A}_{\mathbb{E}} = \begin{bmatrix} -1 & +1 & +1 & 0 & 0 \\ +1 & -1 & 0 & +1 & 0 \\ 0 & 0 & 0 & 0 & +1 \\ 0 & 0 & -1 & -1 & -1 \end{bmatrix},$$

$$\mathbb{A}_{\mathbb{L}} = \begin{bmatrix} -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & -1 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix},$$

$\mathscr{R} = \text{diag}(0, R, 0, 0, 0), \mathscr{L} = \text{diag}(0, 0, 0, L_1, L_2), \mathscr{C} = \text{diag}(C_1, 0, C_2, 0, 0)$.

Define as *manifest variables* (see Sidebar 2) the $|\mathbb{L}|$-dimensional vectors of leaf currents I and of leaf potentials P, and as *latent variables* (see Sidebar 2) the $|\mathbb{E}|$-dimensional vector of edge currents $I_{\mathbb{E}}$ and the $|\mathbb{V}|$-dimensional vector of vertex potentials $P_{\mathbb{V}}$. Explicitly,

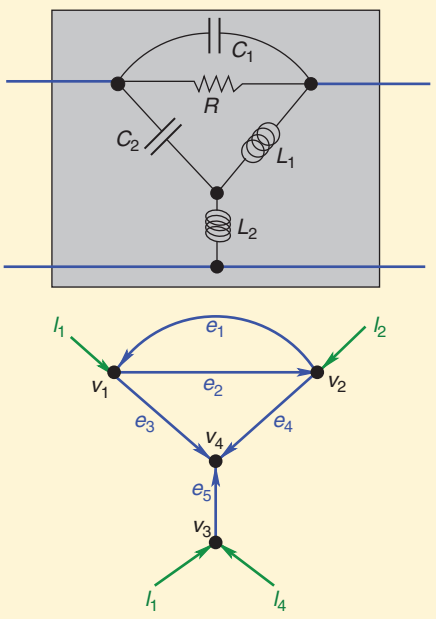


Figure 17. Example circuit and associated digraph with leaves.

$$I = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{|\mathbb{L}|} \end{bmatrix}, \quad P = \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_{|\mathbb{L}|} \end{bmatrix},$$

$$I_{\mathbb{E}} = \begin{bmatrix} I_{e_1} \\ I_{e_2} \\ \vdots \\ I_{e_{|\mathbb{E}|}} \end{bmatrix}, \quad P_{\mathbb{V}} = \begin{bmatrix} P_{v_1} \\ P_{v_2} \\ \vdots \\ P_{v_{|\mathbb{V}|}} \end{bmatrix}.$$

Choosing as latent variables the edge currents and the vertex potentials, as we do here, is the basis of what in circuit modeling is called *modified nodal analysis*.

Define the $|\mathbb{E}| \times |\mathbb{E}|$ diagonal real polynomial matrices $\mathscr{Z}(\xi)$ and $\mathscr{Y}(\xi)$ as follows. The i-th diagonal element of $\mathscr{Z}(\xi)$ equals the diagonal element of $\mathscr{R} + \mathscr{L}\xi$ if this diagonal element is $\neq 0$, and 1 otherwise. The i-th diagonal element of $\mathscr{Y}(\xi)$ equals the diagonal element of $\mathscr{C}\xi$ if this diagonal element is $\neq 0$, and 1 otherwise. The circuit equations can be written explicitly as

$$\begin{aligned} \mathscr{Z}\left(\frac{d}{dt}\right) I_{\mathbb{E}} &= \mathscr{Y}\left(\frac{d}{dt}\right) A_{\mathbb{E}}^{\top} P_{\mathbb{V}}, \\ A_{\mathbb{E}} I_{\mathbb{E}} + A_{\mathbb{L}} I &= 0, \\ P + A_{\mathbb{L}}^{\top} P_{\mathbb{V}} &= 0. \end{aligned} \tag{CE}$$

These equations define the current/potential terminal behavior of the circuit as

$$\begin{aligned} \mathscr{B}_{\mathrm{IP}} = \{(I, P) : \mathbb{R} \to \mathbb{R}^{|\mathbb{L}|} \times \mathbb{R}^{|\mathbb{L}|} \mid \text{there exists} \\ (I_{\mathbb{E}}, P_{\mathbb{V}}) : \mathbb{R} \to \mathbb{R}^{|\mathbb{E}|} \times \mathbb{R}^{|\mathbb{V}|} \text{ such that equations (CE) hold}\}. \end{aligned}$$

(CE) consists of linear algebraic equations corresponding to the resistors, to KCL for the vertices, and to the potential assignment for the leaves, and of first order differential equations corresponding to the inductors and the capacitors. (CE) is a hence set of constant-coefficient linear differential equations. Consequently, it is possible to eliminate the variables $(I_{\mathbb{E}}, P_{\mathbb{V}})$ from equations (CE) and obtain a polynomial matrix F such that $F(d/dt)\begin{bmatrix} I \\ P \end{bmatrix} = 0$ describes the terminal behavior $\mathscr{B}$ (see Sidebar 2). In general, a combination of graph theory ideas and polynomial matrix algebra techniques is used to carry out this elimination, but we do not pursue this further here.

These modeling techniques are readily generalized to other situations than linear RLC circuits. The crucial assumption required is that the circuit elements involve only 2-terminal (multi-)ports. The equations can be adapted to take into account nonlinear elements, elements as transformers, gyrators, etc. However, the method is not suited for modeling circuits containing, for example, 3-terminal 1-ports. We return to this issue in Section 10.

The problem with the use of digraphs without leaves for specifying the architecture of an electrical circuit is that it requires to pair the external terminals in order to define edges that link the external terminals. While, as discussed in Section 4, this is fine for 2-terminal circuits, it causes difficulties for circuits with more than 2 terminals. The pairing imposes the condition that the currents that flow into the circuit along paired terminals sum to zero. This condition unfortunately does not follow from the physics of the circuit, as discussed in Section 6. Moreover, this pairing is an impossibility for circuits with an uneven number of terminals (as transistors, Y's, and Δ's). Usually this is resolved by adding new terminals, often contrary to the physics of the circuit. Digraphs with leaves resolve these dilemmas. Digraphs for describing the circuit architecture and N-ports for describing the interaction of a multi-terminal circuit with its environment are examples of mathematics leading, rather than following, physics.

9. Ports and RLC Circuits

Let $e_{\mathbb{L}} \in \mathbb{R}^{|\mathbb{L}|}$ denote $e_{\mathbb{L}}^{\top} = [1 \quad 1 \quad \cdots \quad 1]$, and use the notation $e_{\mathbb{E}} \in \mathbb{R}^{|\mathbb{E}|}$ analogousy. Note that $e_{\mathbb{E}}^{\top} A_{\mathbb{E}} = 0$ and $e_{\mathbb{E}}^{\top} A_{\mathbb{L}} + e_{\mathbb{L}}^{\top} = 0$.

(CE) implies KCL. Indeed, (CE) implies $e_{\mathbb{L}}^{\top} I = -e_{\mathbb{E}}^{\top} A_{\mathbb{L}} I = e_{\mathbb{E}}^{\top} A_{\mathbb{E}} I_{\mathbb{E}}$. Therefore KCL, $e_{\mathbb{L}}^{\top} I = 0$, follows.

(CE) also implies KVL. Indeed (CE) implies that for all $\alpha : \mathbb{R} \to \mathbb{R}$, $P + \alpha e_{\mathbb{L}} + A_{\mathbb{L}}^{\top}(P_{\mathbb{V}} + \alpha e_{\mathbb{E}}) = P + A_{\mathbb{L}}^{\top} P_{\mathbb{V}}$, which shows that $(P + \alpha e_{\mathbb{L}}, \ P_{\mathbb{V}} + \alpha e_{\mathbb{E}})$ satisfies the third equation of (CE) if $(P, P_{\mathbb{V}})$ does. Further, $A_{\mathbb{E}}^{\top}(P_{\mathbb{V}} + \alpha e_{\mathbb{E}}) = A_{\mathbb{E}}^{\top} P_{\mathbb{V}}$ shows that this also holds for the first equation of (CE).

We now come to the main result of this section. We prove that if the circuit graph is connected and if all the resistors, inductors, and capacitors are > 0, then the only port is the one that consists of all the terminals. Note that the assumption that all the R's, L's, and C's are non-zero can be made without loss of generality. Assume further that each vertex has at most one leaf that is incident with it, and that the edges and leaves are numbered such that edge e_k is incident with leaf ℓ_k for $k = 1, 2, \ldots, |\mathbb{L}|$. Then $A_{\mathbb{L}} = [-\mathrm{id}_{\mathbb{L}} \ \ 0]$, where $\mathrm{id}_{\mathbb{L}}$ denotes the $|\mathbb{L}| \times |\mathbb{L}|$ identity matrix. Partition $P_{\mathbb{V}}$ as $P_{\mathbb{V}} = \begin{bmatrix} P \\ P_{\mathrm{internal}} \end{bmatrix}$. Equations (CE) then become

$$\mathscr{Z}\left(\frac{d}{dt}\right) I_{\mathbb{E}} = \mathscr{Y}\left(\frac{d}{dt}\right) A_{\mathbb{E}}^{\top} \begin{bmatrix} P \\ P_{\mathrm{internal}} \end{bmatrix}, \begin{bmatrix} I \\ 0 \end{bmatrix} = A_{\mathbb{E}} I_{\mathbb{E}}.$$

Our proof of the port property is based on the exponential responses. Take $\lambda > 0$, and define $I^{\lambda} : t \mapsto e^{\lambda t}\alpha$, $P^{\lambda} : t \mapsto e^{\lambda t}\beta$, $I_{\mathbb{E}}^{\lambda} : t \mapsto e^{\lambda t}\gamma$, and $P_{\mathrm{internal}}^{\lambda} : t \mapsto$

$e^{\lambda t}\delta$, with $\lambda \in \mathbb{R}, \lambda > 0$, $\alpha, \beta \in \mathbb{R}^{|\mathbb{L}|}, \gamma \in R^{|\mathbb{E}|}$, and $\delta \in \mathbb{R}^{|\mathbb{V}|-|\mathbb{L}|}$. $I^\lambda, P^\lambda, I^\lambda_{\mathbb{E}}, P^\lambda_{\text{internal}}$ satisfy (CE) if and only if

$$\gamma = Y_{\mathbb{E}}(\lambda)A_{\mathbb{E}}^\top \begin{bmatrix} \beta \\ \delta \end{bmatrix}, \quad \begin{bmatrix} \alpha \\ 0 \end{bmatrix} = A_{\mathbb{E}}\gamma,$$

with $Y_{\mathbb{E}}(\lambda) = (\mathcal{R}^\# + \mathcal{L}^\#\lambda^{-1} + \mathcal{C}\lambda)$, and $\mathcal{R}^\#$ and $\mathcal{L}^\#$ the diagonal matrices that have respectively the inverse of the nonzero diagonal elements of $\mathcal{R}$ and $\mathcal{L}$ in the corresponding entry, and 0 otherwise. Observe that $Y_{\mathbb{E}}(\lambda)$ is a diagonal matrix with positive elements on the diagonal. The above equation leads to the following relation between the exponential responses of the terminal behavior:

$$\begin{bmatrix} \alpha \\ 0 \end{bmatrix} = \begin{bmatrix} Y_{1,1}(\lambda) & Y_{1,2}(\lambda) \\ Y_{1,2}(\lambda)^\top & Y_{2,2}(\lambda) \end{bmatrix} \begin{bmatrix} \beta \\ \delta \end{bmatrix},$$

where $Y(\lambda) = A_{\mathbb{E}}Y_{\mathbb{E}}(\lambda)A_{\mathbb{E}}^\top$ has been partitioned into its first $|\mathbb{L}|$ and last $|\mathbb{V}| - |\mathbb{L}|$ rows and columns. Computation of the matrix $Y(\lambda)$ reveals that its off-diagonal elements are equal to minus the direct admittance between the corresponding vertices. Specifically, the (i,j)-th element of $Y(\lambda)$ for $i \neq j$ equals $-R^{-1}$, $-(L\lambda)^{-1}$, or $-C\lambda$ if there is one edge incident with the vertices v_i and v_j containing the resistor of value R, inductor of value L, or capacitor of value C, the sum of these if there is more than one edge incident with the vertices v_i and v_j, and 0 if there is no edge incident with the vertices v_i and v_j. The (i,i)-th element of $Y(\lambda)$ equals to the sum of the off diagonal elements in the i-th row or the i-th column.

The matrix $Y(\lambda)$ is a symmetric matrix with nonnegative diagonal elements, nonpositive off-diagonal elements, and whose rows (and columns) sum to zero. These matrices (sometimes called symmetric hyperdominant with zero excess) have special properties. In particular, if the circuit graph is connected, then $Y(\lambda)$ has rank $|\mathbb{V}|-1$, and all its principal square submatrices of dimension $< |\mathbb{V}|$ are nonsingular. This implies, in particular, that $Y_{2,2}(\lambda)$ is nonsingular. Further, the left kernel of $Y(\lambda)$ is the span of $e_{\mathbb{V}}^\top$.

These properties of $Y(\lambda)$ can be used to prove that for a connected RLC circuit with positive elements the only port is that consisting of all the terminals. Let $a \in \mathbb{R}^{|\mathbb{L}|}$. Assume that $(I,P) \in \mathcal{B}_{\mathbb{IP}}$ implies $a^\top I = 0$. We wish to prove that that a must be in the span of $e_{\mathbb{L}}$, since then the only port is that consisting of all the terminals. Applying $a^\top I = 0$ to the exponential responses implies that $a^\top(Y_{1,1}(\lambda) - Y_{1,2}(\lambda)Y_{2,2}(\lambda)^{-1}Y_{1,2}(\lambda)^\top) = 0$. From this identity, it follows that $[a^\top - a^\top Y_{1,2}(\lambda)Y_{2,2}(\lambda)^{-1}]$ is in the left kernel of $Y(\lambda)$, and hence in the span of $e_{\mathbb{V}}^\top$. Therefore a is in the span of $e_{\mathbb{L}}$.

Summarizing, we proved the

Theorem: *For a linear RLC circuit that is connected and has all its elements > 0 the only port is that consisting of all the terminals.*

10. Hierarchical Modeling of Circuits

The modeling method discussed in Section 8 is very effective for circuits with elements that consist of 2–terminal ports. Unfortunately, these techniques cannot easily deal with, for example, 3-terminal elements as transistors, Y's, or Δ's, nor can they deal with subcircuits that have already been modeled but contain external terminals that cannot be paired into 2-terminal ports, as, for example the circuits shown in Figures 8, 17, and, as we have seen in Section 9, every connected RLC circuit with more than 2 external terminals. In this section we put forward a modeling methodology that avoids these shortcomings and that is moreover hierarchical in nature.

Consider an interconnected system that consists of interconnected subsystems (for example, the circuit shown in Figure 16). The interconnection architecture of the interconnected circuit can be viewed as a graph with leaves with subsystems in the vertices, connections in the edges, and external terminals as leaves. A model of the external behavior can then be obtained by combining the behavioral equations for the terminal variables of the subsystems in the vertices and the interconnection equations for the edges. This idea allows to model hierarchically, since the interconnected system can in turn be used as a subsystem in a higher hierarchical modeling layer. This idea of modeling by *zooming, tearing, and linking* is explained for general interconnected systems in [8].

In the case of circuits, the interconnection architecture is formalized as a digraph with leaves. The vertices correspond to subcircuits, the edges to the interconnected terminals of the subcircuit, and the leaves correspond to the external terminals. The direction of an edge indicates when the current flowing through the edge is counted as > 0. We assume further that each leaf is directed towards the vertex it is incident with. This is in keeping with our convention that the current in an external terminal is > 0 when it flows into the circuit.

There are $|\mathbb{V}|$ subcircuits, one for each vertex. Denote the subcircuits as $v_1, v_2, \ldots, v_{|\mathbb{V}|}$, and denote the number of terminals of subcircuit v_k by d_k (in the digraph, d_k is actually the degree of vertex v_k). The subcircuit v_k defines a dynamical system $(\mathbb{R}, \mathbb{R}^{d_k} \times \mathbb{R}^{d_k}, \mathcal{B}_k)$ with $\mathcal{B}_k$ the current/potential behavior of subcircuit v_k. In order to specify to which leaves and edges the terminals of subcircuit v_k correspond, we introduce the *leaf assignment*

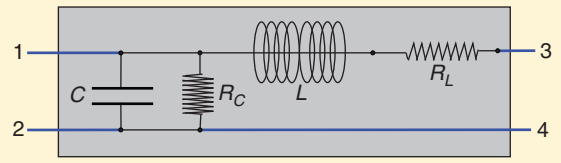


Figure 18. One section of the transmission line of Figure 8.

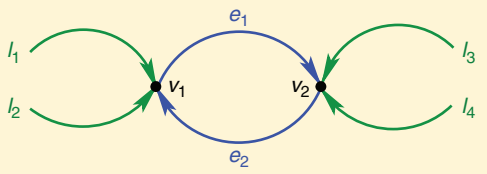


Figure 19. Digraph with leaves for the transmission line architecture.

matrix $A_k^{\mathbb{L}}$ and the *edge assignment matrix* $A_k^{\mathbb{E}}$. $A_k^{\mathbb{L}}$ is a matrix with d_k rows and $|\mathbb{L}|$ columns. Its elements are 0 or $+1$, with the (i, j)-th element equal to $+1$ if the i-th terminal of circuit v_k corresponds to leaf ℓ_j, and 0 otherwise. $A_k^{\mathbb{E}}$ is a matrix with d_k rows and $|\mathbb{E}|$ columns. Its elements are 0, $+1$, or -1, with the (i, j)-th element equal to $+1$ if the i-th terminal of circuit v_k corresponds to edge e_j and vertex v_k is a sink for edge e_j, -1 if the i-th terminal of circuit v_k corresponds to edge e_j and vertex v_k is a source for edge e_j, and 0 otherwise. Denote by $|A_k^{\mathbb{E}}|$ the matrix obtained from $A_k^{\mathbb{E}}$ by replacing all -1's by $+1$'s.

Define as *manifest variables* (see Sidebar 2) the $|\mathbb{L}|$-dimensional vectors of leaf currents I and of leaf potentials P, and as *latent variables* (see Sidebar 2) the $|\mathbb{E}|$-dimensional vectors of edge currents $I_{\mathbb{E}}$ and of edge potentials $P_{\mathbb{E}}$. Explicitly,

$$I = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{|\mathbb{L}|} \end{bmatrix}, \quad P = \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_{|\mathbb{L}|} \end{bmatrix}, \quad I_{\mathbb{E}} = \begin{bmatrix} I_{e_1} \\ I_{e_2} \\ \vdots \\ I_{e_{|\mathbb{E}|}} \end{bmatrix}, \quad P_{\mathbb{E}} = \begin{bmatrix} P_{e_1} \\ P_{e_2} \\ \vdots \\ P_{e_{|\mathbb{E}|}} \end{bmatrix}.$$

The behavior of the interconnected circuit is obtained by combining the behaviors $\mathcal{B}_k$ into

$$\mathcal{B}_{\text{IP}} = \{(I, P) : \mathbb{R} \to \mathbb{R}^{|\mathbb{L}|} \times \mathbb{R}^{|\mathbb{L}|} \mid \text{there exist } (I_{|\mathbb{E}|}, P_{|\mathbb{E}|}) : \mathbb{R} \to \mathbb{R}^{|\mathbb{E}|} \times \mathbb{R}^{|\mathbb{E}|} \text{ such that } (A_k^{\mathbb{L}} I + A_k^{\mathbb{E}} I_{\mathbb{E}}, A_k^{\mathbb{L}} P + |A_k^{\mathbb{E}}| P_{\mathbb{E}}) \in \mathcal{B}_k \text{ for } k = 1, 2, \ldots, |\mathbb{V}|\}.$$

In the linear time-invariant differential case with subcircuit v_k governed by

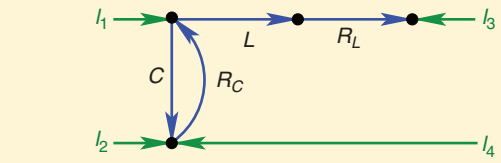


Figure 20. Digraph with leaves for the RLC circuit of Figure 18.

$$R_k^I\left(\frac{d}{dt}\right) I_{v_k} + R_k^P\left(\frac{d}{dt}\right) P_{v_k} = 0,$$

we obtain the behavioral equations

$$\begin{bmatrix} R_1^I(\frac{d}{dt})A_1^{\mathbb{L}} \\ R_2^I(\frac{d}{dt})A_2^{\mathbb{L}} \\ \vdots \\ R_{|\mathbb{V}|}^I(\frac{d}{dt})A_{|\mathbb{V}|}^{\mathbb{L}} \end{bmatrix} I + \begin{bmatrix} R_1^P(\frac{d}{dt})A_1^{\mathbb{L}} \\ R_2^P(\frac{d}{dt})A_2^{\mathbb{L}} \\ \vdots \\ R_{|\mathbb{V}|}^P(\frac{d}{dt})A_{|\mathbb{V}|}^{\mathbb{L}} \end{bmatrix} P + \begin{bmatrix} R_1^I(\frac{d}{dt})A_1^{\mathbb{E}} \\ R_2^I(\frac{d}{dt})A_2^{\mathbb{E}} \\ \vdots \\ R_{|\mathbb{V}|}^I(\frac{d}{dt})A_{|\mathbb{V}|}^{\mathbb{E}} \end{bmatrix} I_{\mathbb{E}} + \begin{bmatrix} R_1^P(\frac{d}{dt})|A_1^{\mathbb{E}}| \\ R_2^P(\frac{d}{dt})|A_2^{\mathbb{E}}| \\ \vdots \\ R_{|\mathbb{V}|}^P(\frac{d}{dt})|A_{|\mathbb{V}|}^{\mathbb{E}}| \end{bmatrix} P_{\mathbb{E}} = 0. \quad \text{(CE')}$$

The linear constant-coefficient differential equation that governs (I, P) can then be obtained by eliminating $(I_{\mathbb{E}}, P_{\mathbb{E}})$ from (CE').

As an example, we consider the circuit of Figure 8 in some detail. We view this circuit as the interconnection of two identical copies of the 4-terminal circuit of Figure 18. The interconnection architecture is shown in Figure 19. The digraph with leaves has 2 vertices, 2 edges, and 4 leaves. Moreover $d_1 = 4$ and $d_2 = 4$. Zooming in on each of the vertices yields, in the obvious notation, the assignment matrices

$$A_1^{\mathbb{L}} = \begin{bmatrix} +1 & 0 & 0 & 0 \\ 0 & +1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}, \quad A_1^{\mathbb{E}} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ -1 & 0 \\ 0 & +1 \end{bmatrix},$$

$$A_2^{\mathbb{L}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & +1 & 0 \\ 0 & 0 & 0 & +1 \end{bmatrix}, \quad A_2^{\mathbb{E}} = \begin{bmatrix} +1 & 0 \\ 0 & -1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}.$$

Assume that the circuit of Figure 18 is governed by

$$R_I\left(\frac{d}{dt}\right) I + R_P\left(\frac{d}{dt}\right) P = 0.$$

For the case at hand, $R_I, R_P \in \mathbb{R}[\xi]^{4\times 4}$. (CE') leads to the equations

For a connected RLC circuit the only port is the one that consists of all the terminals.

$$R_I\left(\frac{d}{dt}\right)\begin{bmatrix} I_1 & I_{e_1} \\ I_2 & -I_{e_2} \\ -I_{e_1} & I_3 \\ I_{e_2} & I_4 \end{bmatrix} + R_P\left(\frac{d}{dt}\right)\begin{bmatrix} P_1 & P_{e_1} \\ P_2 & P_{e_2} \\ P_{e_1} & P_3 \\ P_{e_2} & P_4 \end{bmatrix}.$$

Note the effective use that can be made of the fact that we are dealing with an interconnection of two identical subcircuits. In order to obtain a complete model of the transmission line, we need to eliminate the variables $I_{e_1}, I_{e_2}, P_{e_1}, P_{e_2}$ from the above equations and model the subsystem of Figure 18 in order to obtain R_I and R_P. Modeling the subcircuits in the vertices, here the circuit of Figure 18, may be viewed as the hierarchical step in this modeling procedure.

A model of the subsystem of Figure 18 is readily obtained using the methods explained in Section 8. This leads to the digraph with leaves shown in Figure 20. However, we can also view this circuit as an interconnection of subcircuits: two 4-terminal connectors, C, R_C, L, and R_L. This leads to the digraph with leaves shown in Figure 21.

The modeling methodology of the present section views an interconnected circuit as having *elements (subcircuits) in the vertices* and *connections in the edges*. This in contrast with the classical circuit modeling ideas of Section 8, where we have *elements in the edges* and *connections in the vertices*. The former view of an interconnected circuit is hierarchical in nature and allows for example for 3-terminal elements. While it may appear that when applied to RLC circuits, the modeling methodology of the present section leads to more complicated equations, this is actually not the case. The resulting equations are easily seen to be essentially identical.

11. Passivity

The notion of passivity for circuits has been an elusive one. In this section, we propose a simple definition based on the terminal behavior of a circuit.

Consider an N-terminal circuit that satisfies KVL and KCL. Let $\mathcal{B}_{\mathrm{IP}}$ be its current/potential behavior. The circuit is said to be $[\![\text{passive}]\!] :\Leftrightarrow [\![$ for all $(I,P) \in \mathcal{B}_{\mathrm{IP}}$ and for all $t_0 \in \mathbb{R}$, there exists a $K \in \mathbb{R}$ such that

$$-\int_{t_0}^{t}\left(\sum_{k=1}^{N} I_k(t)P_k(t)\right)dt < K \qquad \text{for } t \geq t_0]\!]. \tag{1}$$

This definition states that a circuit is passive viewed from its terminals if at any time only a finite amount of energy can be extracted from it. This notion of passivity is simple and intuitive, and is developed in [9]. It can be shown that $\mathcal{B}_{\mathrm{IP}}$ is passive if and only if the exists an associated function $V : \mathbb{R} \to [0, \infty)$, called a *storage*, such that

$$V(t_2) - V(t_1) \leq \int_{t_1}^{t_2}\left(\sum_{k=1}^{N} I_k(t)P_k(t)\right)dt$$

$$\text{for } (I,P) \in \mathcal{B}_{\mathrm{IP}} \text{ and } t_1 \geq t_2$$

(for a precise statement, see [9, Theorem 5]).

It is easy to see that the usual circuit elements, as resistors, inductors, capacitors, transformers, gyrators, transistors, and memristors, are passive. The interconnection of passive circuits is again passive. In order to see this, it suffices to analyze the interconnection of two terminals (see Figure 14). Interconnection preserves passivity, since passivity implies that for all $(I,P) \in \mathcal{B}_{\mathrm{IP}}$ such that $I_{N-1} + I_N = 0$, $P_{N-1} = P_N$, and for all t_0

$$\int_{t_0}^{t}\left(\sum_{k=1}^{N-2} I_k(t)V_k(t)\right)dt = \int_{t_0}^{t}\left(\sum_{k=1}^{N} I_k(t)V_k(t)\right)dt < K$$

$$\text{for all } t \in \mathbb{R},\ t \geq t_0.$$

As explained in Sidebar 2, a linear time-invariant differential system always admits an input/output representation. For passive circuits, the input/output partition can be made more concrete. The current/potential behavior $\mathcal{B}_{\mathrm{IP}}$ of an N-terminal circuit is said to admit a *hybrid* representation if the terminals can be partitioned into *voltage driven* and *current driven* terminals. For the voltage driven terminals, the corresponding potentials serve as inputs and the currents as outputs, while for the current driven terminals, the corresponding currents serve as inputs and the potentials as outputs. Note that this implies that 'half' of the variables serve as inputs, and

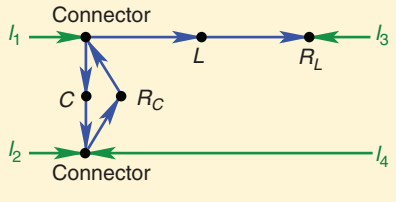


Figure 21. Digraph with leaves for the interconnected circuit of Figure 18.

'half' as outputs. Partition the currents and potentials in accordance with the hybrid nature of the terminals as $I = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$ and $P = \begin{bmatrix} P_1 \\ P_2 \end{bmatrix}$. The existence of a hybrid representation means that a linear time-invariant differential circuit behavior $\mathfrak{B}$ has a kernel representation

$$R_1\left(\frac{d}{dt}\right)\begin{bmatrix} I_1 \\ P_2 \end{bmatrix} = R_2\left(\frac{d}{dt}\right)\begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$$

with $R_1, R_2 \in \mathbb{R}[\xi]^{N\times N}$, and R_1 square and nonsingular. It can be shown [9] that a controllable linear time-invariant differential circuit with such a representation is passive if and only if the associated transfer function $R_1^{-1}R_2 \in \mathbb{R}(\xi)^{N\times N}$ is positive real.

It is easy to verify that resistors, inductors, capacitors, transformers, and gyrators have a hybrid representation. Moreover, it can be shown that the interconnection of passive linear time-invariant differential circuits with a hybrid representation yields again a passive circuit with a hybrid representation. Consequently, large classes of passive circuits have a hybrid representation. The existence of a hybrid representation does not mean that there actually need to be current and voltage sources that drive the external terminals of a circuit.

12. Port-KVL

Consider again the circuit shown in Figure 6 with the first p terminals singled out. We have defined a port in terms of port-KCL, that is, in terms of the currents of the port terminals. This creates an asymmetry between currents and potentials. We now show that for a large class of passive circuits this symmetry can be restored.

$$\Big[\!\Big[\text{Terminals } \{1, 2, \ldots, p\} \text{ are said to satisfy the } \textit{port} - \textit{Kirchhoff voltage law} (\text{port} - \text{KVL})\Big]\!\Big] :\Leftrightarrow$$

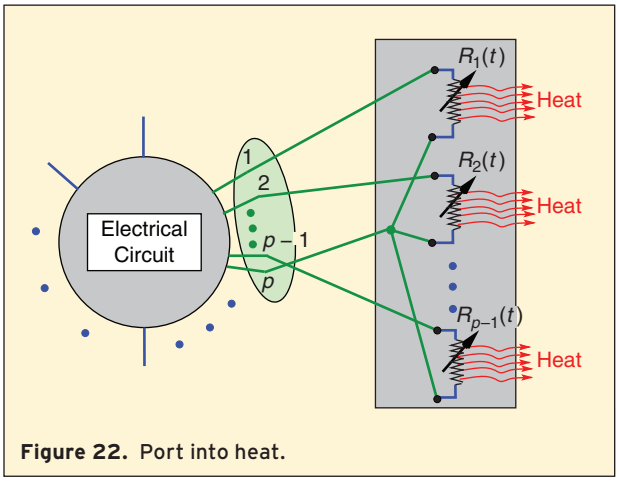


Figure 22. Port into heat.

$$\Big[\!\Big[[\![(I_1, \ldots, I_p, I_{p+1}, \ldots, I_N, P_1, \ldots, P_p, P_{p+1}, \ldots, P_N) \in \mathfrak{B}_{\text{IP}} \text{ and } \alpha : \mathbb{R} \to \mathbb{R}]\!] \Rightarrow [\![(I_1, \ldots, I_p, I_{p+1}, \ldots, I_N, P_1 + \alpha, \ldots, P_p + \alpha, P_{p+1}, \ldots, P_N) \in \mathfrak{B}_{\text{IP}}]\!] \Big]\!\Big]. \qquad \text{(port-KVL)}$$

It follows readily from the results in Section 9 that for RLC circuits, port-KCL and port-KVL are equivalent, since in that case ports consist of all the terminals of connected components. However, the equivalence of port-KCL and port-KVL holds more generally. We have the following result.

Theorem: *Assume that the current/potential behavior of an N-terminal controllable linear time-invariant differential circuit is passive and has a hybrid representation. Then the set of terminals* $\{1, 2, \ldots, p\}$ *satisfies port-KCL if and only if it satisfies port-KVL.*

In order to prove the theorem, assume that the transfer function from input $\begin{bmatrix} P_1 \\ I_2 \end{bmatrix}$ to output $\begin{bmatrix} I_1 \\ P_2 \end{bmatrix}$ is given by

$$G = \begin{bmatrix} G_{1,1} & G_{1,2} \\ G_{2,1} & G_{2,2} \end{bmatrix} \in \mathbb{R}(\xi)^{N\times N}.$$

That it suffices to consider the transfer function for the theorem is a consequence of controllability. Assume that the hybrid representation is 'maximally' voltage driven, meaning that we have chosen as many as possible terminals to be voltage driven. Using positive realness of G, it is readily seen that this implies $G_{2,2} = 0$, for otherwise it is possible to swap some of the output potentials to be inputs instead of outputs. Observe the following equivalence

$$\left[\!\!\left[G = \begin{bmatrix} G_{1,1} & G_{1,2} \\ G_{2,1} & 0 \end{bmatrix} \text{ positive real} \right]\!\!\right] \Leftrightarrow$$

$$[\![G_{1,1} \text{ positive real}, G_{1,2}, G_{2,1} \in \mathbb{R}^{\bullet\times\bullet}, \text{ and } G_{1,2} + G_{2,1}^{\top} = 0]\!].$$

The implication states in particular that $G_{1,2}$ and $G_{2,1}$ are real matrices, rather than rational functions.

We sketch the proof of the theorem by proving a more general statement, namely the following equivalence for $a \in \mathbb{R}^N$:

$$[\![(I, P) \in \mathfrak{B}_{\text{IP}} \Rightarrow a^{\top} I = 0]\!]$$
$$\Leftrightarrow [\![(0, \alpha a) \in \mathfrak{B}_{\text{IP}} \text{ for all } \alpha : \mathbb{R} \to \mathbb{R}]\!].$$

Partition a as $a = \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$, conformably with the hybrid structure of G. There holds

$$[\![(I, P) \in \mathfrak{B}_{\text{IP}} \Rightarrow a^{\top} I = 0]\!]$$
$$\Leftrightarrow [\![a_1^{\top} G_{1,1} = 0 \text{ and } a_1^{\top} G_{1,2} + a_2^{\top} = 0]\!],$$

while

$$[\![(0, \alpha a) \in \mathcal{B} \text{ for all } \alpha : \mathbb{R} \to \mathbb{R}]\!] \Leftrightarrow [\![G_{1,1}a_1 = 0 \quad \text{and} \quad a_2 = G_{2,1}a_1]\!].$$

In order to prove the theorem, it therefore suffices to prove the equivalences

$$[\![\ a_1^\top G_{1,1} = 0\ ]\!] \Leftrightarrow [\![\ G_{1,1}a_1 = 0\ ]\!],$$

and

$$[\![a_1^\top G_{1,2} + a_2^\top = 0]\!] \Leftrightarrow [\![a_2 = G_{2,1}a_1]\!].$$

To show the first equivalence, observe that if, for $M \in \mathbb{R}^{n\times n}$, $M + M^\top \geq 0$ then $[\![Mx = 0]\!] \Leftrightarrow [\![x^\top M = 0]\!]$. Consequently, using positive realness of $G_{1,1}$, there holds $[\![a_1^\top G_{1,1} = 0]\!]$ $\Leftrightarrow [\![a_1^\top G_{1,1}(\lambda) = 0$ for all $\lambda \in \mathbb{R}, \lambda > 0]\!] \Leftrightarrow [\![G_{1,1}(\lambda)a_1 = 0$ for all $\lambda \in \mathbb{R}, \lambda > 0]\!] \Leftrightarrow [\![G_{1,1}a_1 = 0]\!]$. The second equivalence follows immediately from $G_{1,2} + G_{2,1}^\top = 0$.

This yields the desired conclusion and the equivalence of port-KCL and port-KVL.

Note that the above theorem implies in particular the equivalence of port-KCL and port-KVL for a set of terminals of a controllable linear passive circuit that consists of an interconnection of resistors, inductors, capacitors, transformers, and gyrators.

13. Energy

The main concept discussed in this paper is that of a port. We claim that it is only possible to speak about power and energy flow along a set of terminals that forms a port, that is, when port-KCL holds. This statement is of relevance in the discussion of the physics of circuits. The flow of energy involves a number of terminals that are spatially a distance apart. This implies that energy flow is not a local phenomenon, but involves action at a distance.

The aim of this section is to justify the relation between port-KCL and energy flow. Of course, this leads to the question *what is meant by energy*? This query has a somewhat philosophical ring to it and risks to lead to a discussion about the nature of matter and motion. However, this issue must be brought up, since one cannot claim that it is possible or impossible to speak about the flow of energy without explaining what one means by energy. But we will be pragmatic and *define* energy as a physical quantity that can be transformed into heat. We now set out to show how a current/potential trajectory on a port that satisfies port-KCL can be transformed into heat.

Consider first a 2-terminal port. Denote the current into the port by $I = I_1 = -I_2$ and the voltage across the port by $V = P_1 - P_2$. Consider 3 cases: (i) $I(t)V(t) > 0$ for $t \in [t_1, t_2]$, (ii) $I(t) = 0$ or $V(t) = 0$ for $t \in [t_1, t_2]$, and (iii) $I(t)V(t) < 0$ for $t \in [t_1, t_2]$. Assume that $I(t)V(t) > 0$ for $t \in [t_1, t_2]$. Terminate the 2-terminal port by a time-varying resistor with resistance $R(t) = -V(t)/I(t)$. The rate of heat produced by the resistor at time t is $R(t)I^2(t)$, leading to

$$-\int_{t_1}^{t_2} R(t)I^2(t)\,dt = \int_{t_1}^{t_2} I(t)V(t)\,dt = \int_{t_1}^{t_2} [I_1(t)P_1(t) + I_2(t)P_2(t)]\,dt \qquad (\mathscr{E})$$

for the negative of the heat produced in the resistor, and therefore for the energy delivered to the circuit via the port. When $I(t) = 0$ or $V(t) = 0$ for $t \in [t_1, t_2]$, terminate by an open or short circuit. When $I(t)V(t) < 0$ for $t \in [t_1, t_2]$ terminate the port by a source that delivers the current/voltage $(I(t), V(t))$ for $t \in [t_1, t_2]$. Note that this source can be viewed as a negative time-varying with resistance $V(t)/I(t)$. This source, when itself terminated by the time-varying resistance $R(t) = -V(t)/I(t)$, delivers heat to the resistor at the rate $R(i)I^2(t)$, leading to $(\mathscr{E})$ for the energy delivered by the source, and therefore for the energy delivered to the circuit via the port. This yields the desired formulas for the power and energy delivered to a circuit via a 2-terminal port.

Next, consider a p-terminal port. Assume that the current/potential trajectory

$$(I_1, I_2, \ldots, I_p, P_1, P_2, \ldots, P_p) : \mathbb{R} \to \mathbb{R}^p \times \mathbb{R}^p$$

occurs on the terminals of port $\{1, 2, \ldots, p\}$. Port-KCL implies that $I_1 + I_2 + \cdots + I_p = 0$. Now terminate the port by the time-varying resistive circuit shown in Figure 22, with

$$R_1(t) = \frac{P_p(t) - P_1(t)}{I_1(t)}, R_2(t) = \frac{P_p(t) - P_2(t)}{I_2(t)}, \ldots,$$

$$R_{p-1}(t) = \frac{P_{p-1}(t) - P_1(t)}{I_{p-1}(t)}.$$

Note that these time-varying resistances may be positive or negative. In the case that $I_k(t) = 0$ or $P_k(t) = P_p(t)$, interpret the corresponding termination as an open or

closed circuit. It is easily seen that this termination by the time-varying resistive circuit is compatible with the current/potential trajectory at the port, in other words, that this current/potential trajectory can still occur at the port with this termination. Now use the formulas derived in the case of a 2-terminal port to compute the heat dissipated in the positive time-varying resistors or the energy delivered by the negative time-varying resistors viewed as sources. This yields

$$\int_{t_1}^{t_2} [I_1(t)P_1(t) + I_2(t)P_2(t) + \cdots + I_p(t)P_p(t)]\, dt$$

for the energy delivered to the port during the interval $[t_1, t_2]$.

14. Conclusions

We have presented the main concepts of a self-contained introduction to electrical circuit modeling. This material could form the basis for an elementary course in circuit theory. The main novel ideas are the use of a *digraph with leaves* as a formalization of the architecture of an interconnected system such as an electrical circuit, and the notion of a *port* as the fundamental concept for the energy exchange between a circuit and its environment, and between interconnected subcircuits. We also emphasized the difference between *terminals* and *ports*. Interconnection leads to terminals that share their potential and current (up to a sign), while energy transfer occurs through ports. Terminal connection is a *local* operation, while energy involves several terminals simultaneously, and is therefore *action at a distance*.

The notion of a port and the realization that energy exchange is not a local phenomenon, but by necessity involves action at a distance, appears to have been insufficiently emphasized in the literature, in circuit theory as well as in general physics. The idea of using ports as the basic mechanism for energy transfer is presently being extended to other physical domains. For mechanical systems, the notion of a port leads to Kirchhoff's force law, which requires the sum of the forces acting on a system to equal zero. For electrical circuits, the basic building blocks, as resistors, inductors, capacitors, memristors, transformers, gyrators, and transistors, are ports, and so is, therefore, their interconnection. However, in mechanics, springs and dampers are ports, while a mass is not a port. This gives masses a very special role in energy considerations in mechanics.

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