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Silicon germanium based millimetre-wave ICs for Gbps wireless communications and radar systems

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Abstract
This paper establishes the viability and suitability of silicon germanium (SiGe8HP) technology, enablement tools and circuits to millimetre-wave applications today and a roadmap to the future. Key elements discussed include SiGe technology and design enablement advancements leading to the world's most highly integrated, lowest power 60 GHz transmitter/receiver ICs.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Today, existing production level millimetre-wave (mmWave) solutions, e.g. those greater than 50 GHz, utilize bulky packaged III–V components either realized as MCMs or waveguide assemblies with very little integration. What has been missing is an enabling low cost, high volume, 'first time right' technology, which works at mmWave frequencies. This paper will demonstrate that current state of the art SiGe8HP HBT technology, which now demonstrates f_T/f_{max} numbers well above 200 GHz [1–5], with associated gain values greater than 10 dB; figure 1 is capable of such operation and that the enablement tools and models work very well in the millimetre-wave band.

Through this paper we will demonstrate that the models and design tools together with technology can provide a low cost, low power, high yield, high volume solution in which the highest speed communication systems and finest resolution radar and imaging systems can now be manufactured in silicon. As a demonstration and proof point, example record setting integration and lowest power circuit designs for a gigabit-per-second (Gbps) communications link using this technology and these tools will be presented. We will present the underlying technology, enablement tools and finally example circuits.

The framework that underlies this effort consists of SiGe BiCMOS technology (though it could as well be straight CMOS), enabled with both passive and active mmWave capable models and devices. This paper will describe the broad development of the devices undertaken, of which only a subset could be used in the ensuing example. The superset of devices to be described includes mmWave PIN, Schottky and varactor diodes as well as distributed passives e.g. t-lines, couplers, splitters etc.

The block diagram of a multi-Gbps communication system shown in figure 2 is the circuit example for our discussion. The total integration of all elements shown, in SiGe, eliminates all waveguide interconnects and reduces the packaging effort to simple existing high volume packaging technologies.

2. SiGe technology

The commercial success of SiGe technology can be attributed to its ability to provide a very competitive integrated radio solution on a single chip utilizing the high volume manufacturing capability of a standard CMOS processing fabricator. Compound semiconductor technologies, such as GaAs pHEMTs, dominate the millimetre-wave applications today by meeting the critical performance requirements, albeit at a higher cost and lower integration. While these technologies can rival SiGe HBTs for performance, we expect that SiGe BiCMOS technology offers a unique

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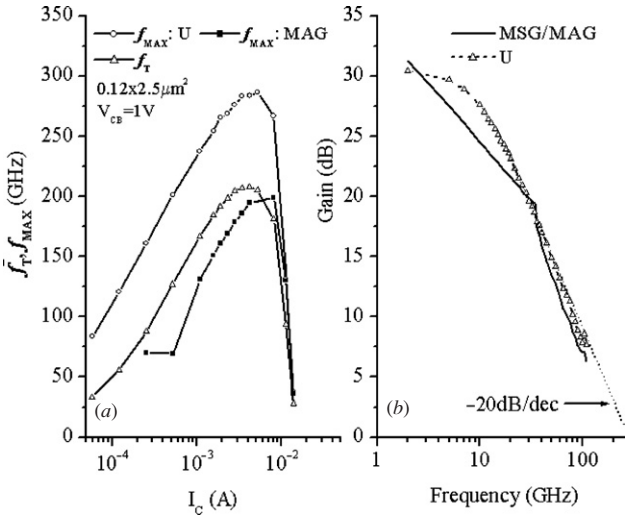


Figure 1. SiGe f_T/f_{max} versus gain.

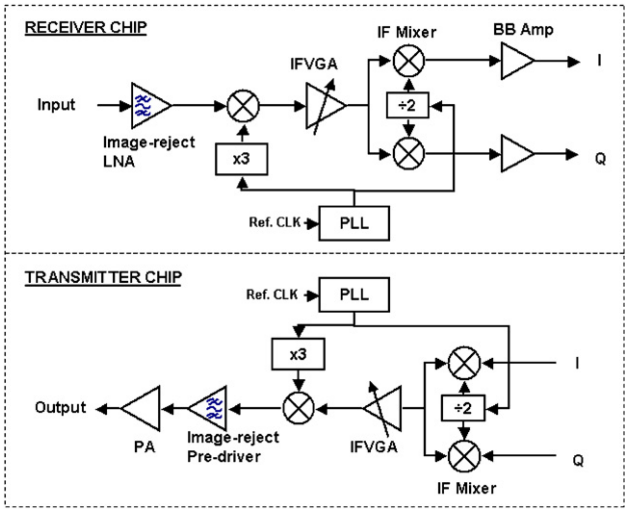


Figure 2. mmWave transceiver block diagram.

potential for mmWave transceiver integration on a chip for low cost and mass market highly integrated applications [6].

The heart of SiGe BiCMOS technology is the SiGe HBT whose f_T/f_{max} performance has been remarkable with a recent report of 300/350 GHz performances [7]. Such bipolar performance can be achieved in the framework of advanced 0.13 μm 8HP BiCMOS integration [8]. The NF_{min} for a 200 GHz f_T transistor built in 8HP is roughly 1.5 dB at 20 GHz, and this can be further improved to adequately meet the mmWave application requirements.

For a fully integrated transceiver solution at mmWave frequencies, SiGe BiCMOS technology needs to address passive as well as active devices e.g. transmission lines for matching, terahertz cutoff frequency Schottky barrier diodes for mixers, low insertion loss PIN diodes for T/R switches, higher resistivity substrates for lower loss and through wafer via-hole features [9].

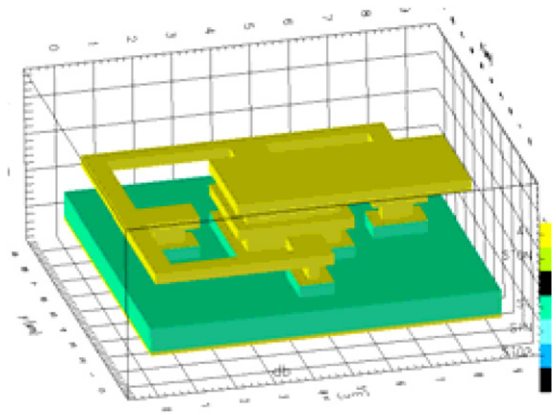


Figure 3. A typical 3D TCAD PIN diode structure used for simulation purposes.

2.1. Active device design enablement

The following active devices are being developed or improved upon for 8HP: the PIN diode, the Schottky diode (SBD) and the vacractor diode. In each case, device optimization was investigated through a series of TCAD simulations, followed by hardware experimentation, and then model development.

For example, figure 3 illustrates a 3D representation of a typical PIN diode, including contacts and wires as well as the dielectric isolation and diffusions. Such complete physical representations were found necessary in some cases to accurately match simulation to experimental data. TCAD allows faster feedback on process and layout optimization actions, and also reveals aspects such as current distribution and relative contribution of various parasitics that may be difficult to obtain through experimental approaches. For example, the separation and common run length between the anode and the cathode contacts can be varied extensively, until the optimal layout is found.

Focusing on the PIN diode, the critical performance metrics are insertion loss and isolation. Numerous layouts to reduce the wiring capacitance as well as the intrinsic resistances, and approaches to improve performance, including the introduction of an additional deep n+ region and its ring reach-through contact to form a cathode region, were optimized against complexity and accuracy. Finally, a near intrinsic epi layer was added and optimized.

Generally, improvements in one parameter would result in some degradation to another parameter. Repeated iteration of several process and layout parameters resulted in improvement of both parameters. The result of this is a PIN diode that provides 0.8 dB insertion loss and 15 dB isolation at 60 GHz, figure 4. Further improvements are underway to push the performance yet higher; see [10].

The Schottky barrier diode (SBD) was improved by a similar methodology. The primary SBD figure of merit for this endeavour was the cutoff frequency. The cutoff frequency varies inversely with resistance and capacitance, the product of which must be lowered to improve Fc. Rarely can any capacitive component be reduced without a simultaneous increase in resistance, and similarly resistance improvements come at the cost of increased capacitance.

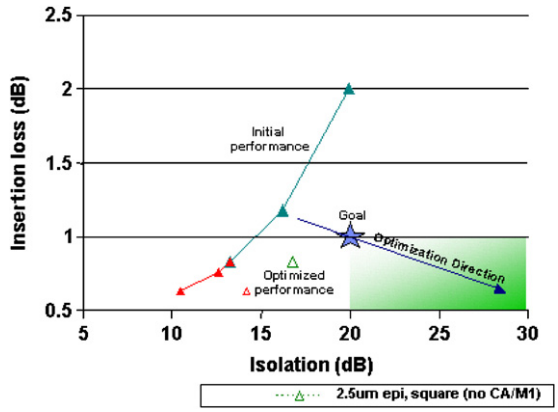


Figure 4. 8HP mmWave (TCAD) 60 GHz PIN diode optimization path.

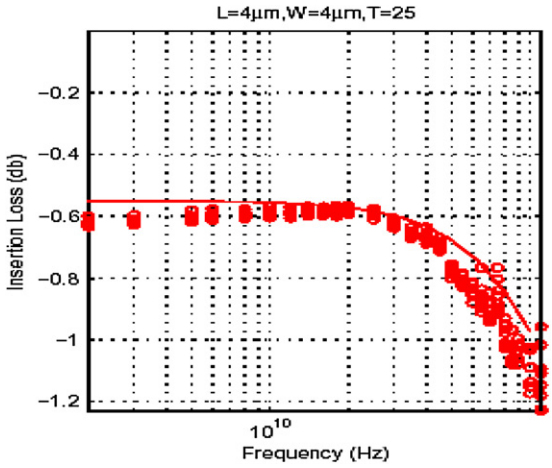


Figure 5. Insertion loss of an isolated 4 × 4 μm PIN diode to 100 GHz: model (line) and measurement (rectangles).

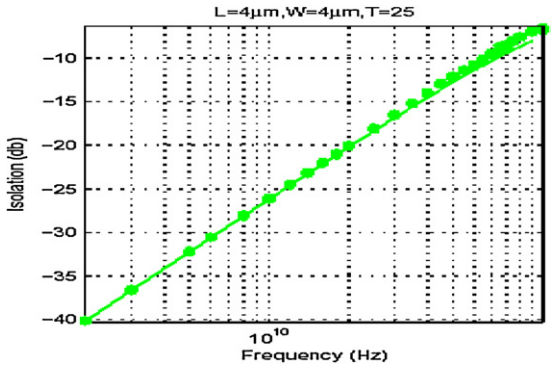


Figure 6. Isolation of a 4 × 4 μm PIN diode to 100 GHz: model (line) and measurement (rectangles). Outstanding model to hardware correlation was obtained.

Thus, the parameters need to be considered jointly for a net improvement.

The dominant parasitics in the SBD are in the Schottky junction itself. Performance gains came primarily from careful selection of the n-type dopant vertical profile both near the surface and far from the junction. Often SBDs are built with various combinations of films and implants introduced into the process primarily for other devices. We have found that dedicating some processing steps to the SBD measurably enhanced the performance. For mmWave applications, the additional processing cost is fairly small relative to the alternatives.

The varactor diode may be realized as either a junction diode or a MOS varactor diode. The MOS version takes advantage of the advanced CMOS processing in the technology, whereas the junction varactor is fabricated primarily by dedicated processing. The two embodiments compete fairly closely in terms of the tunability and quality factor metrics. Various process modifications to enhance both devices are under evaluation, as well as circuit applications to determine the preferred embodiment. The performance achievements made thus far have been through layout—in particular migrating to smaller anode sizes and tighter ground rules.

The SBD and PIN diode share much of the same processing and they share processing with the HBT transistor. Three additional masks permit the fabrication of these two devices. The junction varactor may be realized with one additional mask, though in practice two are used.

Compact device models were created for the PIN diode and varactor using measurements to 100 GHz on early hardware. Device characteristics were de-embedded from scattering parameters using the pad-open-short method assuming perfect standards. The fit of the critical parameters of insertion loss and isolation at 25 °C for the 3 × 3 μm and 4 × 4 μm PIN diodes is good, but the behaviour above 60–70 GHz is likely influenced by incomplete de-embedding of parasitic elements; see figures 5 and 6. The model scales well over this range and to larger devices. Smaller devices may require an even more careful accounting of the three-dimensional nature of the device.

The development of a scalable model allows the circuit designer to tailor the device to his needs. The 4 × 4 μm anode size provides good insertion loss and isolation characteristics for lower frequencies, but may have insufficient isolation at frequencies over 50 GHz. A smaller anode size would significantly improve isolation; insertion loss would increase but remain acceptable.

A FET is an alternative to the PIN diode in an RF switch design. We have investigated this and found FETs to have an unacceptably high insertion loss.

For the varactor model, including the effects of wiring and distributed Nwell resistance enabled the prediction of Q over the range of interest. Again the data are obtained from pad-open-short de-embedding with the assumption of perfect standards and data above 60–70 GHz are likely influenced by incomplete de-embedding of parasitic elements; see figures 7 and 8. An anode finger width of 18 μm is shown here for model-to-hardware correlation. The Q is strongly dependent on the anode dimensions, and smaller anode widths are necessary to achieve our best case results of a Q of 7 at 60 GHz. Including the effects mentioned above, and scaling the epi thickness enabled projection of a Schottky diode model from hardware. The model is consistent with the corner frequency extrapolated from early hardware. SBD and PIN mask costs are expected to be less than a 10% increase, even in this early phase.

Table 1. Device goals/advancements in BiCMOS 8HP technology for the mmWave devices.

Element	Goal	Start	Accomplishment
PIN diode	Iso >–20 dB; IL < 1 dB at 60 GHz	Iso ∼ 6 dB; IL ∼0.6 dB at 60 GHz	Iso = 0.8 dB; IL = 15 dB at 60 GHz
SBD diode	fc > 500 GHz	fc ∼ 200 GHz	fC ∼ 800 GHz
Varactor diode	Q > 10 at 60 GHz	Q ∼ 2 at 60 GHz	Q = 7 at 60 GHz

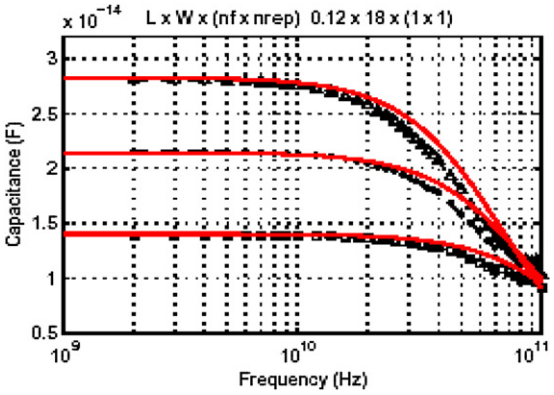


Figure 7. Capacitance of a single long finger varactor model (line) compared to HW measurements (triangles 1.4 V, circles 0.0 V, squares −0.4 V).

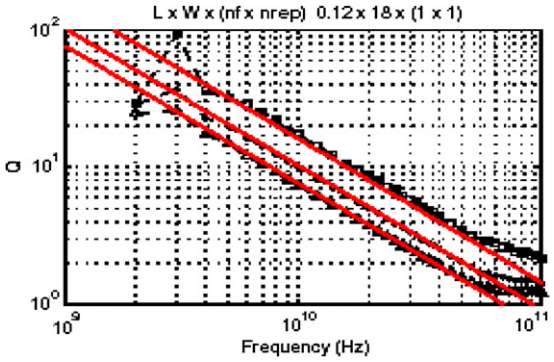


Figure 8. Q of a single long finger and varactor (line) compared to HW measurements (triangles 1.4 V, circles 0.0 V, squares −0.4 V).

Table 1 summarizes the progress attained for these devices with respect to the targeted performance goals. All these new or enhanced mmWave devices/models were enabled in the standard cadence environment.

3. Distributed passive design enablement

Millimetre-wave (mmWave) passive devices include transmission line types such as the microstrip, coplanar waveguide, matching stubs, junction types such as tees, bends, crosses, steps, gaps, and a combination of both types that are constructed to create functional devices such as couplers, power splitters/combiners, baluns, filters and any other passive elements that are required by mmWave circuit designers. The smaller wavelengths of mmWave frequencies make it feasible to integrate such devices on chip. The passive element models are based on distributed elements rather than the lumped element models that are frequency limited by self-resonance at the mmWave frequencies and they account for the skin effect and substrate interaction. This improves the design cycle time by including the parasitics in the model rather than waiting for the layout extraction and re-simulation. Also, the passive element models include the process tolerance and can be simulated statistically. The passive elements are offered as full library devices in a 0.13 μm SiGe BiCMOS Design Kit. This includes a paramterized cell (Pcell), which can be stretched through parameter inputs. The Pcell has schematic symbol views, models and passes design rule check (DRC), and layout versus schematic (LVS) checks.

A hierarchical Pcell is used for the functional distributed passive device, which consists of transmission line and junction element Pcell and sub-circuit models. All models are developed on the basis of electromagnetic (EM) simulations and verified/tuned with measured results.

Figure 9 shows the hierarchical sub-circuit, layout Pcell and schematic symbol of a meander-line Branch coupler, which consists of four tees, four transmission lines and four meander lines. The meander line sub-circuit model consists of nine transmission lines and four corners. All hierarchical distributed passive devices have their own layout Pcells and schematic symbols which allow the designers to generate the layout and run simulation just like any other library devices.

Figure 10 shows a comparison between spectre model simulation, EM simulation (HFSS^{TM}) and measurements for the meander-line branch coupler designed at 60 GHz, for which good correlations have been established.

The transmission line model covers both the microwave (frequency domain) and the high speed digital (time domain) applications. This allows the designers to model all the critical interconnect lines of a given design. Figure 11 shows good correlation between the return loss and the insertion loss of the models versus the EM simulation from dc up to 200 GHz.

Figure 12 shows the tee model simulations versus measurements. In the measurements, the tee is terminated with a 50 Ω resistor to match the two port VNA measurement. In order to make an apples-to-apples comparison, the model simulations included extra microstrip lines to make the total length equal to the measured structure. This resulted in good model to hardware correlation. A similar approach was used for the corner model.

4. Circuit design

The technology and enablement foundation for SiGe circuits working at mmWave frequencies have now been realized as just described and further detailed in [11, 12]. We then exercised a subset of these elements in a gigabit-per-second integrated 60 GHz transmitter (Tx) and complimentary

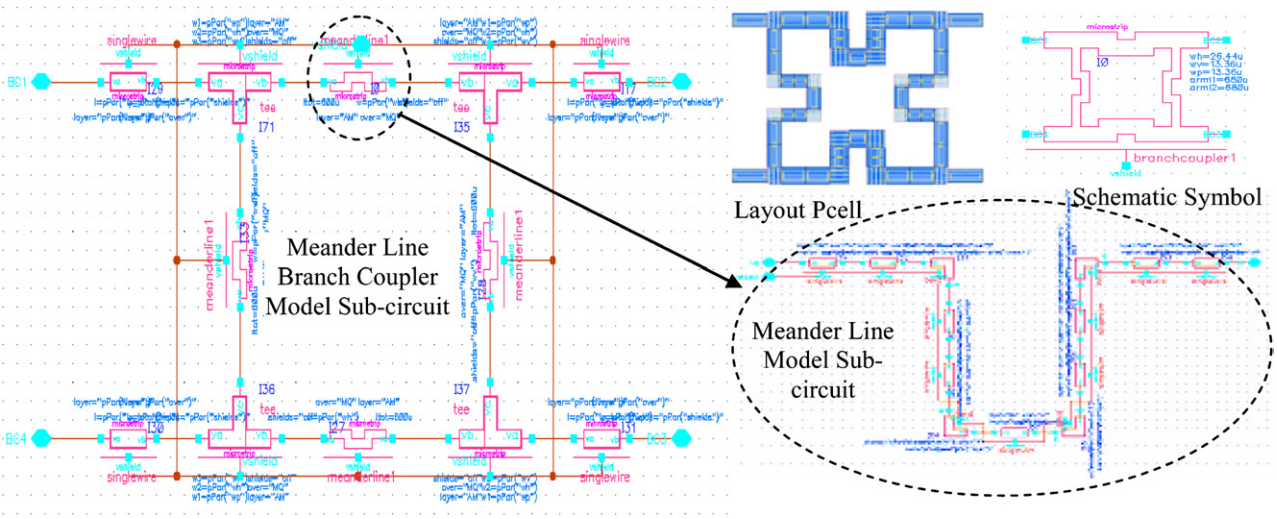


Figure 9. Model sub-circuits for a meander line branch coupler and a meander line.

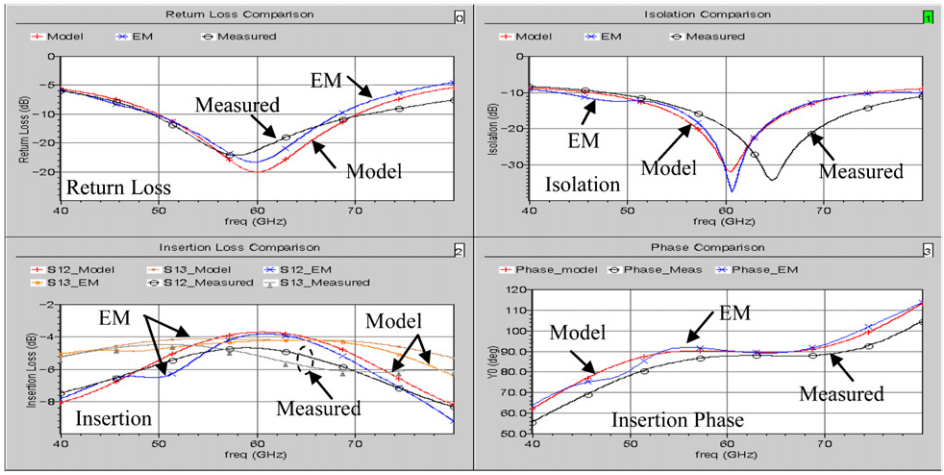


Figure 10. Spectre model, EM simulation and measured data comparison for a 60 GHz meander line branch coupler.

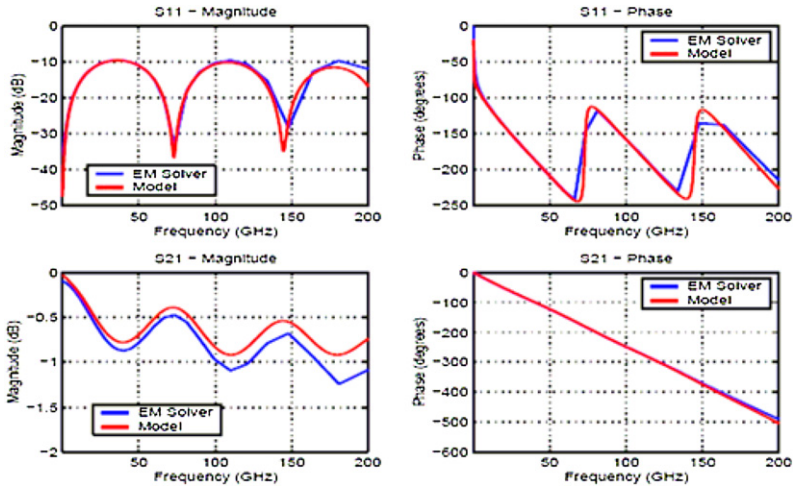


Figure 11. *S*-parameters AM over MQ, $w = 27.5$ μm.

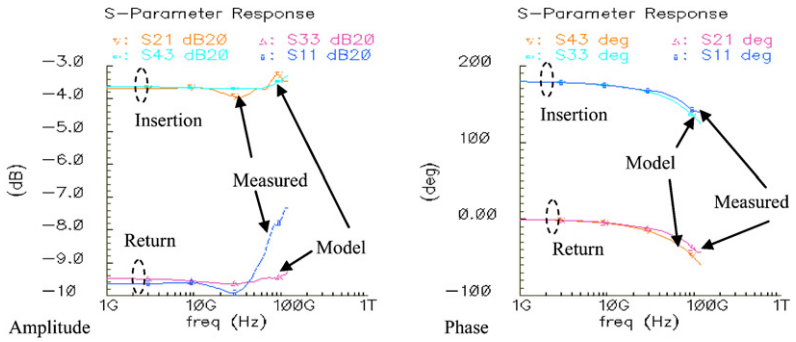


Figure 12. Measured and model simulation comparison.

receiver (Rx) front end, figure 2, to demonstrate these capabilities and prove the value of this work. All RF and analogue portions of the Rx and TX are integrated into two chips. Figure 2 shows the block diagram of the Rx and Tx, which is a conventional superheterodyne architecture with a single LO. This architecture utilized a variable intermediate frequency (IF) to minimize complexity, chip area/cost. The Tx and Rx image rejection is handled on chip, as is IF filtering. Local oscillator signals for the mmWave or IF mixers are generated by either tripling or halving the frequency of the VCO/PLL signal, respectively. For 59–64 GHz operation, this architecture results in an IF of 8.4–9.1 GHz, a VCO frequency of 16.8–18.3 GHz, and an image frequency of 42–46 GHz. Each mmWave block was designed using this new technology and enablement tools previously described. Extensive use was made of the transmission line elements for matching structures, couplers and filters.

LNA measurements across 59–64 GHz show 5–6.2 dB NF, 20 dB gain, <−12 dB S_{11}/S_{22} and <−40 dB S_{12}. Image rejection is >26 dB; i$P_{1\,\mathrm{dB}}$ is −29 dB m; and power consumption is 10 mA from 2.7 V.

The first Rx mixer described in [11, 12] provides about 9 dB of conversion gain. This Rx mixer is followed by an IF variable-gain amplifier (IFVGA) with 0–10 dB of gain, quadrature IF mixers with unity gain, and unity gain baseband output buffers to drive external 100 Ω differential loads. IF filtering centred at 8.8 GHz is provided by the loads of the Rx mixer and IFVGA, with a cascaded IF bandwidth of >±700 MHz. The cascaded NF of the mixer and subsequent stages is 13 dB at 25 °C.

An integer-N PLL is included with the Rx and Tx. The PLL operates off of a 520–610 MHz reference clock, generating a 16.6–19.5 GHz output signal. PLL measurements show a phase noise of −95 to −100 dB c Hz^{-1} at 1 MHz offset with an RMS jitter <1.5° integrated over 1 MHz–1 GHz. The PLL consumes ∼75 mW from 2.7 V and 4 mW from 1.5 V. The local oscillator for the Rx mixer is provided by a harmonic frequency tripler [11, 12]. The tripler output is >560 mVppd at the mixer switches, with phase noise floor <−132 dB c Hz^{-1}.

On-wafer measurements were made on the full Rx with PLL. The Rx power conversion gain is 38–40 dB and the NF is 5–6.7 dB. Image rejection is 30–40 dB and $P_{1\,\mathrm{dB}}$(in) is −36 dB m. The Rx consumes 195 mA from 2.7 V, 50 mA of which is in the baseband output buffer. At 85 °C, NF remains below 8 dB while gain drops 5–6 dB.

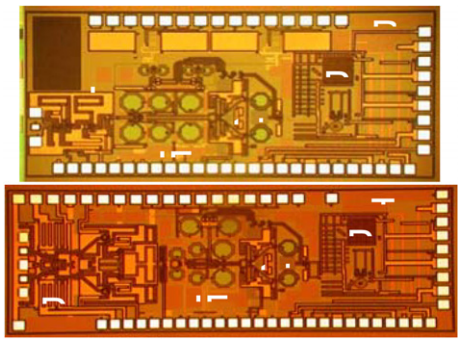


Figure 13. Tx (top) and Rx (bottom) die micrographs.

Shifting to the Tx, the power amplifier (PA), which is a linear, class-AB amplifier that has 15 dB gain at 61.5 GHz. Measurements show a 10.5 dB m output $P_{1\,\mathrm{dB}}$ and >17 dB m P_{sat}. The power-added efficiency (PAE) across the ISM band is between 10 and 6%.

A pre-driver amplifier is included to provide signal amplification and >25 dB image rejection. Measurements on the pre-driver show 8–12 dB of gain and 6–8 dB m output $P_{1\,\mathrm{dB}}$. The circuit consumes 36 mA from 2.7 V.

The IF strip in the transmitter is the reverse of that in the receiver. The IFVGA provides a maximum signal level of −3 dB m at 59–64 GHz to the pre-driver. IF filtering is again provided by the IF mixer and IFVGA loads, with ±700 MHz BW.

We measured output power and conversion gain versus I/Q input power of a 100 MHz CW tone for 59, 61.5 and 64 GHz. $P_{1\,\mathrm{dB}}$ is 10–12 dB m; P_{sat} is 16–17 dB m; and the conversion gain is 34–37 dB. I/Q quadrature accuracy was within ±1°. At $P_{1\,\mathrm{dB}}$, the Tx consumes 190 mA from 2.7 V and 72 mA from 4 V. On-wafer Tx/Rx measurements are summarized in table 2, with circuit detail in [12] and figure 13.

We explored a number of chip-scale packaging options for the Rx and Tx ICs. Folded-dipole antennas were used for both the Tx and Rx modules. Figure 14 shows the Tx chip wire-bonded to an FR-4 circuit board. The antennas are cavity-backed superstrate folded dipole antennas fabricated on fused-silica. The antenna was then flip–chip attached to the Tx chip using gold stud-bumps. Experiments and

Table 2. Measured Tx and Rx performance from 59–64 GHz at 25 °C.

60 GHz receiver measurement		60 GHz transmiter measurement	
Gain	35–40 dB	Gain	34–37 dB
Noise figure	5–6.7 dB	$P_{1\ dB}$ (out)	10–12 dB m
S_{11} RF in	−15 dB	P_{sat}	16–17 dB m
Image rejection	>30 dB	Image rejection	20–30 dB
P_{top} (in)	−35 dB m	PAE of PA	6–10%
IIP3	−30 dB m	Carrier suppression	21–25 dB
3 × LO leakage RF in	<−77 dB m at 52–55 GHz	3 × LO Spur	−25 to −20 dB m
Phase noise	−85 to −90 dB m Hz^{-1}	Phase noise	−85 to −90 dB c Hz^{-1}
(1 MHz tripled)	<−130 dB c Hz^{-1} floor	(1 MHz tripled)	<−130 dB c Hz^{-1} floor
I/Q balance	0–4° < 105	I/Q balance	±2° ± 0.5 dB
Power description	195 mA, 2.7 V	Power description	190 mA, 2.7 V 72 mA, 4.0 V

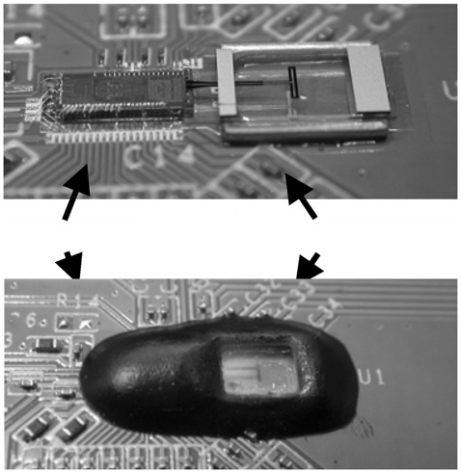


Figure 14. Packaging of 60 GHz chips, before encapsulation (top) and after (bottom).

simulations indicate the Tx antenna efficiency was >95%. The Rx antenna included a wide-band balun [13] on the substrate to match the single-ended Rx LNA input. The Rx antenna gain is also approximately 7 dBi with a beamwidth of ±30°, bandwidth (−10 dB S_{11}) of 20 GHz, and efficiency of >90% [14, 15].

Most of the link measurements were done using these chip-on-board packages, figure 14. We experimented with a number of modulation formats, but for WPAN we settled on a version of the IEEE 802.11a-based OFDM-QPSK modulation at 630 Mb s^{-1} for our demonstration platform because of its robustness at combating multi-path interference due to reflections off the walls, floor and ceiling. The range was defined based upon ⩽10% packet-error rate running at 630 Mbps, which yielded a 10 m separation; a sensitivity defined by the 802.11a standard convention. These measurements support link budget calculations, which suggested a 10 m range with receiver sensitivity of −68 dB m at 630 Mb s^{-1}. These same link budget calculations predict an 8 m range at 1 Gb s^{-1} [16]. The maximum data rate in these experiments was limited by the sampling rate of the ADC, not the Rx and Tx ICs.

5. Conclusion

We described newly developed, enhanced technology, models and enablement features that lead to state of the art mmWave ICs. Die photographs of the Rx and Tx are shown in figure 14. The die sizes are 3.4 × 1.7 mm^2 and 4.0 × 1.6 mm^2, respectively. We also presented the framework for extending this SiGe BiCMOS technology with additional devices and enhancements to new, dual-use application spaces such as wireless communication and advanced radar systems operating at frequencies up to 120 GHz.

The impact of this work will be to enable high volume silicon germanium-based technology to work in the millimetre-wave frequency region. This implies all the advantages of silicon, including high levels of integration, low cost, low power and good thermal characteristics. A key feature of this work is that it includes not only the required technology enhancements, but also the required design environment extensions in a standard cadence design environment.

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