Detailed Analysis of Charge Pumping and I_dV_g Hysteresis for Profiling Traps in SiO_2/HfSiO(N)

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By scanning 1/3 nm SiO_2/HfSiO(N) gate dielectrics with Variable t_{charge}-$t_{discharge}$ Amplitude Charge Pumping technique (VT^2ACP) and slow rate I_dV_g hysteresis, we study in detail the energy profile and estimate the spatial position (within SiO_2 or HK layer) of pre-stress and stress-induced electron traps. Pre-stress traps are mainly at shallow energy levels while stress-induced traps are at deeper energy levels. We demonstrate that due to incomplete discharge of bulk traps, the commonly-used base level charge pumping (CP) sweep is not suited for trap energy profiling. Further, we show that in CP measurements, due to the non-negligible tail of the filling probability of traps, even at short charge times, a fraction of HK-bulk traps is scanned in addition to interfacial traps. When the trap density in the HK is significantly higher than in the IL, this fraction might dominate the CP signal and can cause misinterpretation of data. Finally, we point out the possible contribution of the initially-present traps in the formation of a percolation path causing the dielectric breakdown.

Keywords: Charge pumping, HfSiO(N), energy and spatial distribution of traps

This work is part of IMEC's Industrial Affiliation Program, funded by IMEC's core partners: Intel, Texas Instruments, Micron, Infineon, NXP, ST, Matsushita, TSMC, Samsung and Elpida. Support from IMEC's p-line for processing and AMSIMEC for electrical characterization is greatly acknowledged.

I. INTRODUCTION

Hf-based dielectrics are shown to be potential candidates to replace SiO_2 as the gate dielectric [1]. In recent years a lot of work was performed on characterising the spatial and energetic position of traps in different gate dielectrics, in particular High-K stacks. However, contradictory conclusions [2, 3] regarding the traps responsible for Stress induced Leakage Current (SILC) and breakdown (BD) indicate the necessity of further accurate investigation.

Charge pumping (CP) is an established analysis technique [4, 5] to investigate traps in dielectrics. By varying the CP frequency, different fractions of the trap density can be sensed. It is general knowledge that at high frequencies (short charging times) only traps "very close" to the interface can be sensed. However, the meaning of "high frequency" is vague and can cause erroneous interpretation of data. In this work we illustrate that the filling probability of the traps during CP is not a sharp step profile as a function of the distance from the interface and its non-negligible tail results in the scanning of traps further from the interface than expected.

Further, we demonstrate that due to incomplete discharge of bulk traps, the commonly-used base level sweep CP is not suited for trap energy profiling. In order to investigate the energy profile of the traps accurately, we perform a defect scanning using Variable t_{charge}-$t_{discharge}$ Amplitude Charge Pumping technique (VT^2ACP) [6]. We learn about the difference in energy profile of the initial defects and the generated traps under Constant Voltage Stress (CVS) in HfSiO(N).

Applying a slow variant of I_dV_g hysteresis (20 ms at each V_g-step and waiting 1s at the highest V_g before measuring the down ramp of the sweep) complementary to charge pumping allows us to investigate deeper in the HK bulk to study the spatial profile of defects.

II. DEVICES

The samples characterized in this work are fresh and electrically-stressed HfSiO(N)-based MOSFETs with TiN metal gate fabricated with a conventional self-aligned transistor flow [7]. ~3 nanometer thick $HfSiO_x$ layers with ~80% Hf were deposited by atomic layer deposition (ALD) on a 1 nm thick chemical SiO_x interface layer (imec-clean [8]). The gate stacks were exposed to a soft decoupled plasma nitridation followed by a post-deposition anneal in O_2 in order to maintain an amorphous homogeneous film without phase separation and also to reduce leakage current [9]. Poly-Si capped TiN metal gates were next deposited by ALD. The transistors have EOT=1.55 nm and show state of the art performance.

III. LIMITATIONS OF BASE LEVEL CP

In the basic CP measurement introduced by Brugler and Jespers [10] the drain and the source are connected to ground or to a reverse bias, where a voltage pulse is applied to the gate and the substrate current is measured. Note that in conventional CP theory only interface states are considered [4]. These are sensed during the pulse voltage transients, while states deeper in the oxides are accessed during the constant high and low voltage parts of the pulse.

When the nMOSFET is pulsed into inversion, electrons flow from the source and drain into the channel and traps are filled through tunneling in both the SiO_2 interface layer and the HK bulk. In this paper we define the pulse time in inversion as the "charging time (t_{charge})" at the corresponding charging voltage V_{charge}. When the gate is pulsed into accumulation, mobile electrons of the channel drift back into the drain and source but the trapped electrons recombine with the majority carriers coming from substrate giving rise to a net flow of negative charge into the substrate. It has been shown [11] that due to the large hole barrier, the recombination of electrons at energy levels above the Si conduction band edge and further away from the

substrate mostly happens after the trapped electrons have tunneled back to the substrate. It is also possible that the emitted electrons are collected by the source/drain diffusions and therefore the charge pumping current is always an underestimation of the trap density. However, in our measurements, due to the choice of transistors with long channel length (L=10 μm), a substantial fraction of the emitted electrons recombines with substrate holes and is detected by CP.

We will define the pulse time in accumulation as the "discharge time ($t_{discharge}$)" at the corresponding discharging voltage $V_{discharge}$.

When the HK is separated from the substrate by a thin SiO_2, traps in the HK can be sensed at low frequencies [12, 22, 23]. In order to measure these states, a base-level charge pumping with constant pulse amplitude (schematically shown in Fig. 1) is performed with fixed rise and fall time (200 ns) and variable frequency with a duty cycle of 50%. $V_{discharge}$ (conventionally also called V_{base}) is swept from -2 to 1V.

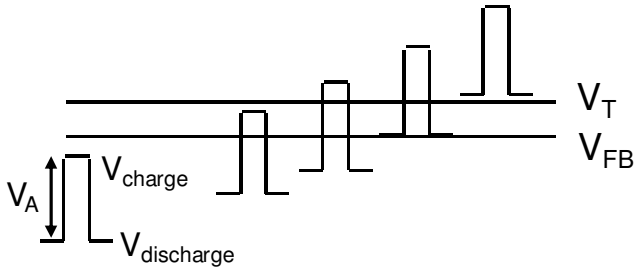

Figure 1: Schematic illustration of the base-level charge pumping with constant amplitude.

Fig.2 shows the traps sensed per area unit obtained from equation (1) on a fresh device.

$$N_{OT}=I_{CP}/qAf \qquad (1)$$

In this equation I_{cp} is charge pumping current, q the electron charge, A the device area and f the frequency.

By decreasing the frequency, we observe, apart from an increase caused by gate leakage current at $V_{discharge}$ < -2V, two distinct peaks at $V_{discharge}$ =~ -0.7V and $V_{discharge}$ =~ 0V. They are

commonly interpreted as being caused by two pre-existing traps with different energy levels. This interpretation is based on the alignment between the electron injection level at V_{charge} and the energy level of the trap. Indeed, at V_{charge} all dielectric traps with energy level below the injection level in the inversion layer that are within reachable distance from substrate can be charged. At increased V_{charge} more shallow traps are accessible due to the increased field. However, the exact levels of the accessed traps depend both on charge time and charge voltage. As will be shown later in section IV, for the considered frequency and limited voltage range, the charging voltage is the dominant parameter determining trap energy, and most measured traps are close to the SiO_2/HK interface.

Assuming the above interpretation is correct, the left peak in Fig. 2 corresponds to energetically deeper traps while the right peak is caused by energetically shallower traps. Note that the shape of the CP-characteristic is not due to any spatial non-uniformity and/or non-uniform degradation (e.g. channel hot hole injection) [13], as the channel length is not short (L=10 μm).

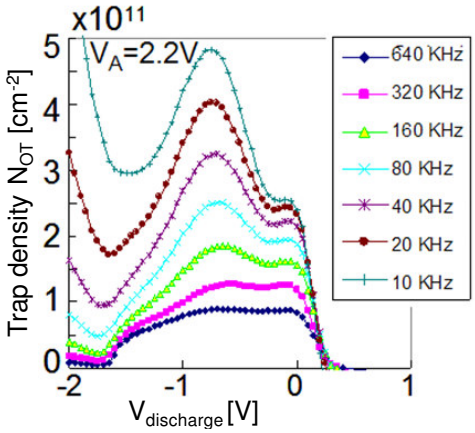

Figure 2: Charge pumping (by sweeping $V_{discharge}$ as illustrated in Fig.1) performed at fixed V_A = 2.2V, t_r = t_f = 200 ns and variable frequency with duty cycle of 50% detects two distinct peaks at $V_{discharge}$ =~ -0.7V and $V_{discharge}$ =~ 0V. The current increase observed at $V_{discharge}$ < -2V is due to the gate leakage current.

The trap generation under Constant Voltage Stress @V_g = 2.7V is further investigated. As shown in Fig.3, the amplitude of the left peak increases with stress time while the right peak does not grow, suggesting no significant generation of energetically shallow traps. By repeating the sequence of stress-CP-stress at room temperature, energetically deep trap generation follows a power law with exponent ~0.3, as shown in the inset of Fig.3. Note that the shift in the right edge of the CP signal after stress indicates charge trapping. This will be confirmed in section V.

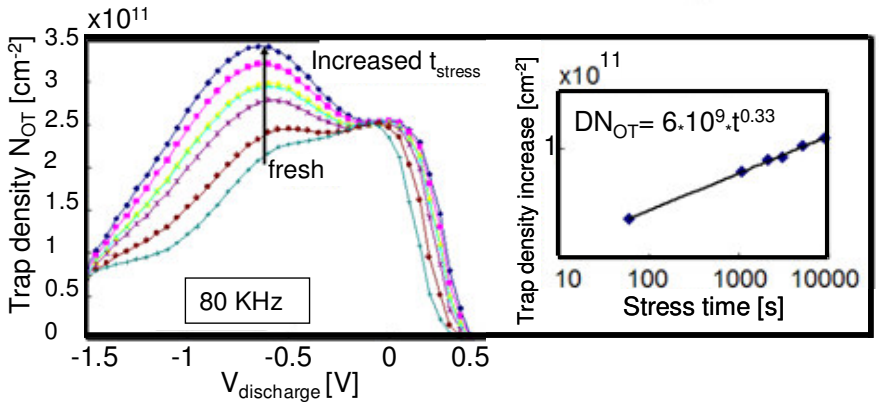

Figure 3: Trap generation under CVS (V_g = 2.7V) measured by CP. The amplitude of the left peak increases with stress while the right peak does not grow. The left peak representing the energetically deep traps has a trap generation rate of ~0.33.

By increasing the amplitude of the gate pulse V_A to $V_A+\Delta V_A$, it is possible to scan traps in a wider energy range. CP measurements by applying square pulses with different amplitudes (from 1.4 V to 2.2 V) at a frequency of 120 kHz are shown in Fig.4. In the range where CP is possible ($V_{discharge} < V_{fb}$ and $V_{discharge}+V_A > V_T$), it is expected that by increasing V_A to $V_A + \Delta V_A$, the same traps are measured at $V_{discharge} - \Delta V_A$, causing a shift of the CP-curve to the left over an interval ΔV_A. If the peak positions in the CP-curve were only determined by the alignment of the electron injection level at charging voltage $V_{charge} = V_{discharge} + V_A$ to the energy level of the defects, these peak positions would also shift to the left over ΔV_A.

Surprisingly, in Fig.4 by changing the pulse amplitude, no obvious shift in the peak positions is observed. In order to explain this discrepancy, we have to revisit the simple explanation given earlier. Each point of the CP curve is the steady state current generated by all electron traps that are charged and discharged during each gate pulse. However, during the transient phase preceding steady state, incomplete discharge occurs, causing an unbalance between trapped and de-trapped charges. Although each point of the CP current curve in Fig.4 corresponds to the steady state value, each steady state is reached at a different amount of the remaining un-discharged traps.

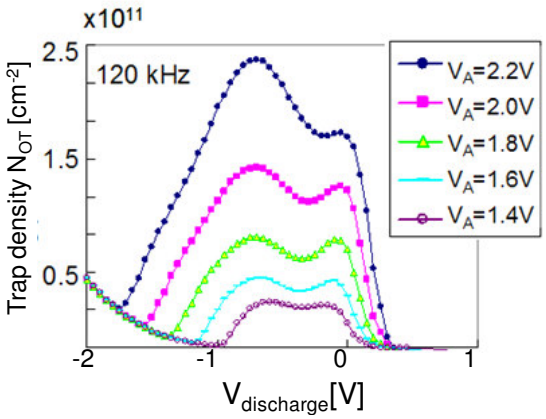

Figure 4: Base level charge pumping performed at variable V_A= 1.4 V to 2.2 V. By changing the pulse amplitude, no obvious shift in the position of the peaks is observed. The slight difference in the shape of the fresh CP curve in Fig.3 and this figure is due to a different sample choice.

With the schematic shown in Fig.5, we explain how the CP signal is affected by the balance between charge trapping and de-trapping. The solid lines are CP data from Fig. 4 and the dashed lines are a schematic drawing of the possible underlying trap density. Also a schematic drawing of the transient discharge probability is shown in the bottom figure. We focus on the CP peak of Fig.4 at ~ $V_{discharge}$ = -0.7V and define two regions: region 1 at $V_{discharge} < V_{peak}$ and region 2 at $V_{discharge} > V_{peak}$. In region 1, $V_{discharge}$ is sufficiently low to guarantee a complete charging and

discharging in each CP pulse. The increase of the CP current as a function of $V_{discharge}$ therefore reflects a true increase in measured trap density. In agreement with this interpretation, the CP signal at increasing V_A shifts to the left over the interval ΔV_A as expected. In region 2, however, $V_{discharge}$ is insufficient to guarantee complete discharge of trapped electrons and consequently, the steady state CP current shows only a fraction of the real trap density. As $V_{discharge}$ increases, this fraction decreases resulting in a decreasing CP current. In summary, the peak in Fig.5 is created by the transition from the complete to the incomplete discharge. This transition depends on the discharge voltage and discharge time but is only weakly dependent on the amplitude V_A.

We point out some causes of the incomplete discharge (during transient) in a frequency sweep at constant duty cycle. As shown in [14], the deviation of the measured energy of electrons from the calculated energy in elastic tunneling is caused by the inelastic nature of the trapping process.

The energy relaxation of the traps results in a slower discharging compared to charging. Also, in the classical base level CP as shown in Fig.1, the increase of the $V_{discharge}$ causes an insufficient discharge field which results in residual charges in the stack. These factors make a complete discharge in the simple frequency sweep with constant duty cycle difficult if discharge voltage and/or discharge time are insufficient.

In order to extract the defects energy profile, an independent control of charging and discharging is necessary. Variable t_{charge}-$t_{discharge}$ Amplitude CP, presented in the next section, is a modified CP technique that solves the incomplete discharging issue.

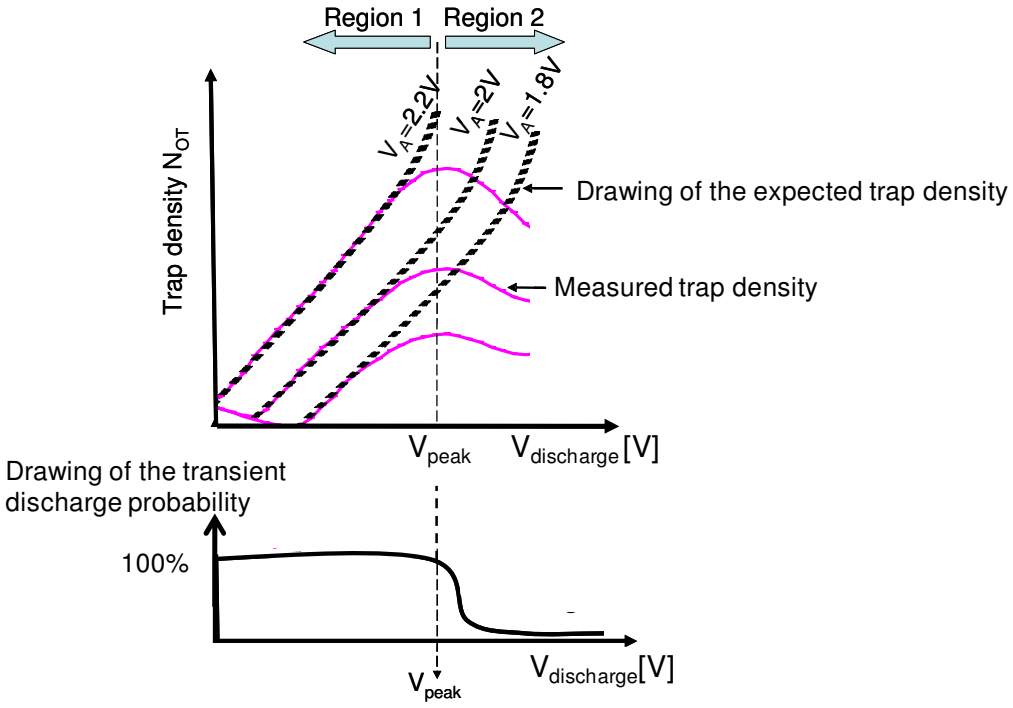

Figure 5: Schematically drawing of how the CP signal is affected by the balance between charge trapping and de-trapping. In the top figure, the solid lines are CP data from Fig. 4 and the dashed lines are a schematic drawing of the possible underlying trap density. A schematic drawing of the transient discharge probability is shown in the bottom figure. In region 1, $V_{discharge}$ is sufficiently low to guarantee a complete charging and discharging in each CP pulse. The CP signal at increasing V_A shifts to the left over the interval ΔV_A. In region 2, however, $V_{discharge}$ is insufficient to guarantee complete discharge of trapped electrons. The peak is created by the transition from the complete to the incomplete discharge.

IV. TRAP ENERGY PROFILE WITH VT^2ACP

For an accurate investigation of the energy profile of the traps, we perform Variable t_{charge}-$t_{discharge}$ Amplitude Charge Pumping (VT^2ACP) [6]. With this technique we independently control the trap charge and discharge condition. The measurement sequence is shown in Fig.6: We apply a gate pulse with constant $t_{discharge}$ and constant $V_{discharge}$. Several amplitude sweeps at

increasing t_{charge} are taken. We emphasize that by choosing a long $t_{discharge}$ = 100 µs at favorably negative $V_{discharge}$ = -0.7 V, the possibility of incomplete discharge due to trap relaxation and/or unfavorable discharge voltage is suppressed at any charging condition. This will be confirmed further by the observed increased trap density as function of V_{charge} in Fig.8.

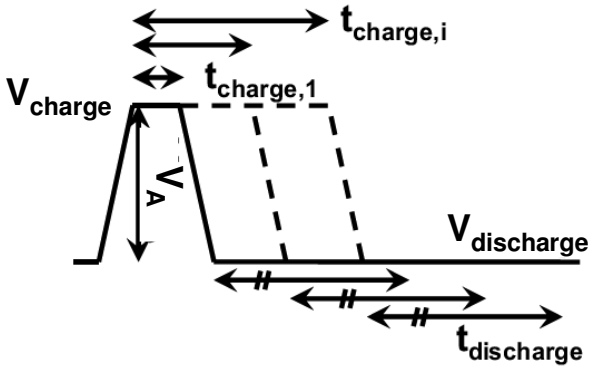

Figure 6: Schematically drawing of the pulse applied in VT^2ACP. A gate pulse with constant $t_{discharge}$ and constant $V_{discharge}$ is applied. Several amplitude sweeps at increasing t_{charge} are taken.

With VT^2ACP, by varying t_{charge} and V_A, simultaneous scanning of the distance to the interface and energy levels of traps is possible. The transformation from (t_{charge},V_A) to (x,E) is not straightforward. We assume that traps are filled by direct tunneling from the inversion layer through the oxide barrier. The methodology used to calculate the filling probability of the traps is elaborated in detail in a separate paper and will here be limited to a brief summary:

The occupation probability of traps (filling probability) is given by

$$f_T = 1 - \exp[-c_n \cdot t_{charge}]. \qquad (2)$$

which is divided into $f_{T,SiO2}$ and $f_{T,HK}$. The electron capture rate (c_n) in equation (2) is determined by the capture cross section of electrons (σ_n), the bouncing frequency (f_b) of electrons to the interface in the inversion layer [15], the electron concentration in silicon conduction band at inversion ($n_{n,C.B.}$), and the probability of direct tunneling calculated with

Wentzel-Kramers-Brillouin (WKB) approximation [16]:

$$c_n = \sigma_n f_b n_{n,C.B.} T_{WKB}(x, V_{gate}) \quad (3)$$

The tunneling probability using the WKB approximation is a function of scanning distance (x) and applied gate voltage (V_{gate}). As capture cross section, we assumed a constant value which represents an average effective value of the exponentially decreasing electron-capture probability as function of the difference between injection level and trap energy level. The uncertainty induced by this simplification is not pronounced as e.g. the extracted trap level difference in Al_2O_3 [17] with and without accounting for electron relaxation was seen to be only ~ 0.2eV, providing the capture cross-section is properly calibrated.

For fixed gate voltage and t_{charge}, the filling probability varies from 100% (all traps occupied) to 0% (totally empty) as a function of distance to the substrate interface. We define the scanned distance as the distance for which the filling probability equals 50%.

The results at t_{charge} = 10 µs and 100 µs for V_G= 0.8V as a function of the distance from the interface are shown in Fig.7a. At 50% filling probability and t_{charge} = 100 µs, traps at the distance of 0.96 nm from Si/SiO_2 interface are scanned. This is almost at the interface between SiO_2 and HK.

In Fig.7b, the filling probability calculated for t_{charge} = 100 µs at V_G = 0.8V and 1.2V (corresponding with the extremes in our measured voltage range) is shown. At 50% of these two filling probabilities, only ~0.2 nm difference in the scanning distance (0.96×10^{-9}m at 0.8V and 1.18×10^{-9}m at 1.2V) is observed. We have calculated that the difference in energy level for V_G=1.2V at 0.96×10^{-9}m and 1.18×10^{-9}m is only 0.03eV. Compared to the scanned energy range of 0.3eV, corresponding to gate voltage range, we approximately make 10% error on the trap energy when neglecting the voltage effect on scanning distance. In the remainder of this paper we can therefore safely assume that all traps are at the SiO_2/HK interface and V_{charge} can be mapped directly into an energy w.r.t HK-Conduction band edge as shown in Fig.8b, bottom axis.

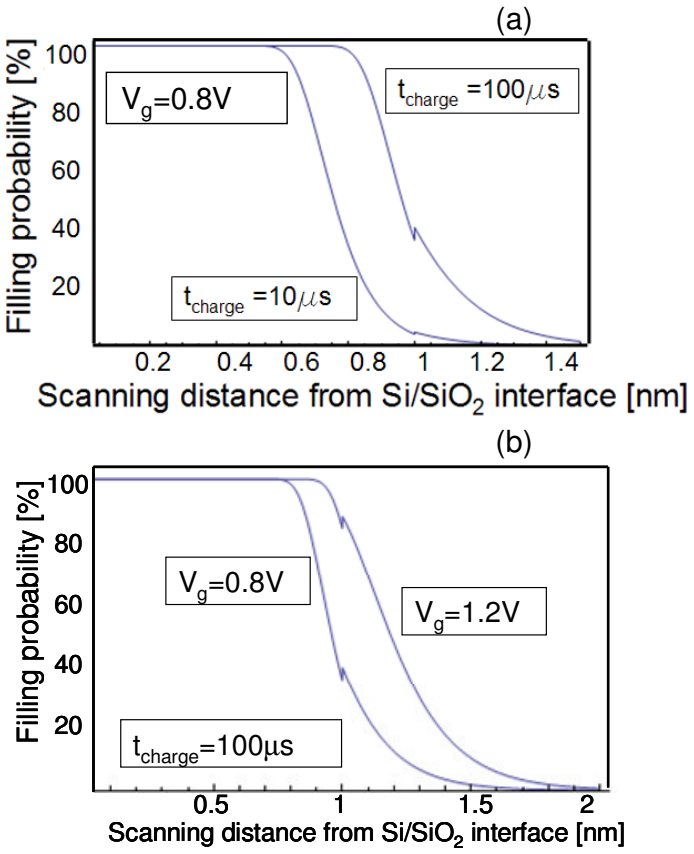

Figure 7: (a) Calculated filling probability for t_{charge} = 10 µs and 100 µs and V_g = 0.8V is not a sharp step function and at t_{charge} = 10 µs, a non-negligible tail reaches up to a distance of 1.2 nm from the Si/SiO_2 interface (b) Filling probability calculated for t_{charge} = 100 µs at V_G = 0.8V and 1.2V (corresponding with the extremes in our measured voltage range). Note that the discontinuity observed at 1 nm of the scanning distance from Si/SiO_2 interface is due to the change of the physical parameters of SiO_2 (e.g. effective mass) to HK parameters.

Fig.8a shows the trap density as a function of the charging voltage V_{charge} at different t_{charge} from 1 µs to 100 µs on a fresh device. By subtracting the trap density measured at low t_{charge} (1 µs) from the trap density at higher t_{charge} (10 µs or 100 µs), we exclude both the Si/SiO_2 interface traps (i.e. the "classical" charge pumping component [4, 5]) and all traps in SiO_2 with

charging times shorter than 1 µs and obtain the trap density profile near the SiO_2/HK interface. The same procedure is also applied on the stressed devices. Taking the derivative with respect to the voltage, results in the trap density profile shown in Fig.8b (fresh). Additionally the change of this profile after CVS at 2.7 V and increased stress time is shown (ΔD_{OT} in Fig. 8b). We verified that the gate leakage current was sufficiently small in the entire CP measurement range shown in Fig. 8b.

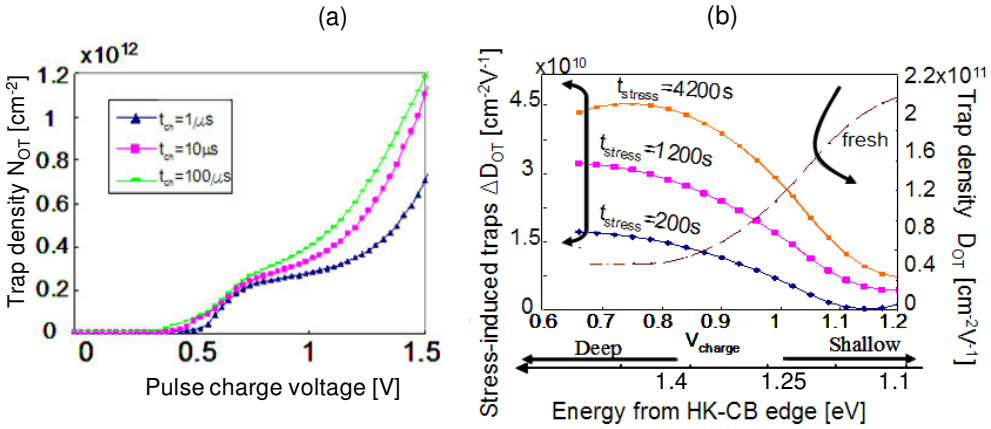

Figure 8: (a) shows the trap density versus V_{charge} on a fresh device obtained from VT^2ACP at different t_{charge} from 1 µs to 100 µs. In this measurement fall and rise times were chosen sufficiently long (t_r = t_f = 100 ns) to avoid geometric component. (b) The fresh curve (representing initial defects) reveals a constant density in the deep energy levels and a continuous increase of density in the shallow energy range. After CVS (V_g = 2.7V), the trap density increase is maximal at deep energy levels.

As presented in Fig.8b, the fresh curve (representing initial defects) reveals a constant density in the deep energy levels and a continuous increase of density in the shallow energy range (with a possible maximum at 1.1 eV). This confirms that: 1) the decrease of CP signal for $V_{discharge}$ > -0.7V in Fig.2 is indeed due to incomplete discharging and justifies the schematic drawing in Fig. 5. 2) the peak at $V_{discharge}$ ~ 0V in Fig.2 is also a result of the measurement method and caused

by a continuously increasing signal cut off by the switch-off of the CP operation at $V_{discharge} = V_{fb}$.

It is also shown in Fig.8b that after CVS, the trap density increase is maximal at deep energy levels ~ 1.4 eV below the HfSiO(N) CB edge. The stress-induced trap density follows a power law as a function of time with exponent 0.3 confirming our previous results in Fig.3. Since the energy level of the stress-induced traps differs from the energy level at which the maximum density of the initial defects occurs, these defects have a different microscopic nature.

After further investigation of Fig.7, we observe that the filling probability is not a sharp step function and for example at t_{charge} = 10 µs for V_{charge} = 0.8V, a non-negligible tail reaches to a scanning distance of 1.2 nm from the Si/SiO_2 interface, i.e. inside the HK. This means that even at short charge times a part of electrons can be captured inside the HK. If the trap density in the HK is significantly higher than in the IL, this fraction might even dominate the CP signal. This result has to be taken into account when interpreting CP results. This is even more pronounced at higher charge times and voltages. The simple reasoning that at short charge time the scanning distance is limited to interfacial layer only, is absolutely incorrect.

Finally, even at low frequency (long charge time about a few ms), VT^2ACP scans only traps until ~1.2 nm from the interface (50% filling probability) [18]. In order to study the traps further away from the substrate interface, we need a complimentary scanning technique and therefore in the next section we investigate the hysteresis in the I_dV_g curve.

V. TRAP SPATIAL PROFILE BASED ON I_DV_G HYSTERESIS

In a conventional hysteresis measurement a quasi DC ramp is applied to the transistor. When charge trapping/de-trapping is present, the initial trace will deviate from the final trace due to build up or loss of charge.

To study the spatial position of the traps, we investigate charge trapping monitored by I_dV_g

characteristics with V_d = 0.1 V when sweeping from accumulation towards inversion and back, while successively increasing the maximum gate voltage $V_{g,max}$. We apply sufficiently negative gate bias i.e. -1V to obtain complete charge recovery after each sweep. Instead of measuring I_dV_g as fast as possible to ensure maximum hysteresis, we deliberately chose a `slow` sweep (20 ms at each V_g-step using an Agilent 4156) and we wait 1s at the highest V_g before measuring the down ramp of the sweep. In such a slow ramp measurement, de-trapping during the down trace is much more pronounced compared to fast measurements with μs ramp rates as e.g. in pulsed I_dV_g [19]. Due to the fast-transient discharging behavior in conventional DC measurement and surely the choice of very long charging (discharging) time (20ms) in our measurement, it is guaranteed that the measured hysteresis is caused by defects present in the central part of the HK. Note that the magnitude of the voltage-shifts is extremely small as the full impact of trapping cannot be captured by the conventional DC measurements [19].

To reduce the inaccuracies on the extracted voltage-shifts, we have recently developed a new analysis technique which allows to model the entire I_dV_g hysteresis curve with so-called least squares support vector machines (LS-SVM) [20] without loosing accuracy in the curved part around threshold voltage. Based on this model, we developed a constrained optimization problem resulting in the extraction of maximum hysteresis. The details of this technique will be published in a separate paper [21]. The maximum ΔV for I_dV_g sweeps with increasing $V_{g,max}$, is a measure for trap density and is shown in Fig.9 for fresh and stressed devices. A continuous increase of the hysteresis on fresh devices is observed at higher V_g. Generally, this increase can be either due to a larger injection probability due to the larger electric field and/or a larger contribution of shallow states for larger gate voltages. However, inspired by the results of VT^2ACP (in previous section) detecting energetically shallow traps on the interface between SiO_2 and HK, we speculate that also the HK traps causing the increase of hysteresis at high V_g are shallow.

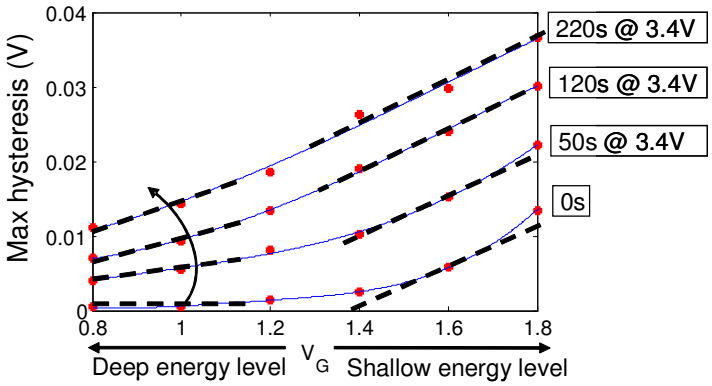

Figure 9: shows the extracted maximum ΔV from slow rate I_dV_g sweeps with increasing $V_{g,max}$ in fresh and stressed devices. The underlying curves serve as guide for the eye. The fresh curve reveals a continuous increase of the hysteresis and of the trap density possibly in the shallow energy level range. After CVS, the maximum trap density increase is observed at deep energy levels.

After CVS, the maximum trap density increase (corresponding with maximum change in tangent-slope between fresh and post-stress) is observed at deep energy levels. Note that after stress, the hysteresis indicates no significant increase in trap density in high V_g range since the tangent-slopes are almost parallel in this range. These observations are in excellent agreement with CP results found in previous section (Fig.8b).

The results presented in this paper reveal a potential misinterpretation of Time Dependent Dielectric Breakdown (TDDB) data. If only the stress-induced traps are correlated with Breakdown, one neglects the possible role of the initially- present traps in the formation of a percolation path. As shown schematically in Fig.10, the initially-present defects can participate in the percolation path, while additional deep traps need to be generated with CVS to make the path complete. Also this situation is comparable with a two-layer stack where one layer is initially "full" of defects (already broken) and additional traps are needed to break the remaining layer. Only considering the role of the layer with newly generated defects results in incorrect

conclusions regarding the cause of breakdown.

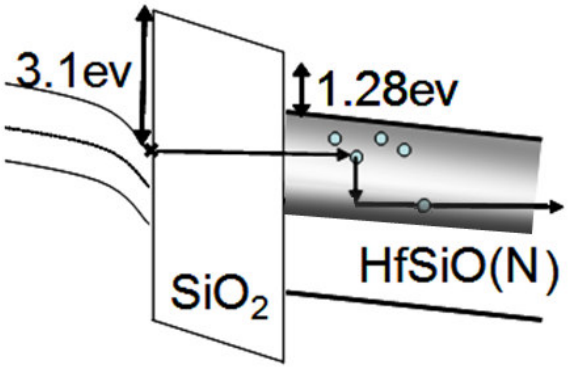

Figure 10: Schematically illustration of how the initially-present defects can participate in the percolation path, while additional deep traps need to be generated with Constant Voltage Stress (CVS) to make the path complete.

VI. CONCLUSIONS

We have studied in detail the energy distribution of the electron traps and estimated their spatial position in a 1/3 nm SiO_2/HfSiO(N) gate dielectric. We demonstrated that the commonly used base level sweep charge pumping can yield erroneous interpretation because of incomplete discharge of traps. Variable t_{charge}-$t_{discharge}$ Amplitude Charge Pumping having a long discharge time and the slow rate I_dV_g hysteresis show the true trap profile. In summary, on fresh samples, the defect density increases in the shallow energy range, while traps generated by CVS reach a maximum density at deep energy levels. Furthermore, we have pointed out two matters of caution that can lead to misinterpretation of data: 1) in CP, due to the non-negligible tail of the filling probability, even at short charging times (high frequencies), a fraction of HK-bulk traps is scanned. When the trap density in the HK is significantly higher than in the IL, this fraction might dominate the CP signal. 2) Initially present defects can participate in the percolation path, while additional traps need to be generated (e.g. with CVS) to make the path complete.

Neglecting the contribution of initial defects can result in incorrect conclusions regarding the cause of breakdown.

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