HfSiO Bulk Trap Density Controls the Initial V_{th} in nMOSFETs

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***Abstract*—The underlying physical mechanism of V_{th}-adjustment of nMOSFETs with HfSiO/TiN gate stack obtained by As and Ar implantation is investigated. It is experimentally proved that the trapped charge in the HfSiO bulk defects controls the initial V_{th} in nMOSFETs. Reduction of the charged trap density in HfSiO by implant explains the tuned V_{th}-values.**

***Index Terms*—initial V_{th},V_{fb}, HfSiO bulk Defect density, reliability**

I. Introduction

AGRESSIVE scaling of the gate oxide in complementary metal oxide silicon (CMOS) transistors has resulted in an unacceptably high gate leakage current. This is explained as the SiO_2 layer is scaled to a thickness range where direct tunnelling through the potential barrier of the insulator is the dominant conduction mechanism. To achieve a lower leakage current at the same equivalent oxide thickness (EOT), there has been high interests in the implementation of Hafnium-based dielectric/metal gate stacks (having higher dielectric constant) as replacement of traditional SiO_2/poly-Si gate stacks [1]. However, a major issue that must be addressed is the MOSFET threshold voltage (V_{th}) and flatband voltage (V_{fb})-control, which depends on the metal work function and the interactions between metal and dielectric.
Several techniques are capable of adjusting V_{th} as for example the use of capping layers such as La, Sc, Er or Sr [2], implantation [3] and introducing impurities such as N, P, F [4].

Providing a physical explanation for these V_{th}-adjustment techniques has been the goal of frequent studies [5, 6, 7]. Cartier *et al.* [8] suggested that the V_{th}/V_{fb} modulation is caused by the variation of the oxygen vacancy concentration in the high-k near the metal contact. Due to an electron charge transfer from the oxygen vacancy to the metal electrode, an accumulation of positive charge at the high-k side and accumulation of negative charge at the metal side occurs. Consequently, the formed dipole results in upward bending of the bands at the dielectric side and hence change of the effective gate work function and therefore the V_{th}/V_{fb} modulation is observed. Based on their model, they also suggest that the V_{th}/V_{fb} shift can be recovered by removal/passivation of the oxygen vacancies at low temperatures or by annealing in O_2 which results in the reduction of the charge transfer between the metal/dielectric interface and hence decrease of the dipole. Other authors [2, 9, 10] suggested that the interface between high-k and SiO_2 interface layer plays an important role in the effective work function modulation. They claim that the formation of a highly polar bond, for example a La-O bond, creates a dipole. Consequently, the local potential drop due to this dipole between the SiO_2 interface layer and the high-k modifies the V_{th}/V_{fb}.
Despite the numerous studies, the underlying physical mechanism of the V_{th}/V_{fb}-tuning methods is not unambiguously understood.

In this paper we study the V_{th}/V_{fb} reduction by implantation of either Arsenic (As) [3] or the inert Argon (Ar) [11] which are both viable options for making metal gate CMOS integration meet the targets specified in the ITRS roadmap [12]. The focus of this paper is not on the processing aspects of the implantation technique, but we investigate the physical part and the underlying mechanism of this V_{th}/V_{fb} adjustment technique.

In Section II, we discuss the results obtained by As gate implantation and review a model from Singanamalla *et al.* [7] explaining the V_{th}/V_{fb} -adjustment by As gate implantation based on an induced dipole at the metal/high-k interface modulating the metal work function. At this point, we reveal the incapability of the proposed model to explain the V_{th}/V_{fb}-adjustment by implantation of an inert species such as Ar.
In Section III, we provide an in-depth study of the underlying physical mechanism of V_{th}/V_{fb}-tuning by gate implantation and propose a new model challenging the dipole models in the literature. Applying electrical defect characterization techniques, in Section IV we experimentally prove that the trapped charge in the high-k bulk defects controls the initial V_{th}/V_{fb} in nMOSFETs. Further in Section V, we provide chemical analysis and a 3D reconstruction of the studied structures and reveal the role of Nitrogen (N) in adjusting the V_{th}/V_{fb} values when As or Ar are implanted through the gate. In order to complete the study, in Section VI, we investigate the reliability aspects of the implanted compared to the non-implanted reference devices by performing PBTI and TDDB tests and we explain how to interpret the results of the reliability tests based on the trap characterization outcomes. Finally in Section VII, we summarize the paper.

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II. V_{TH}/V_{FB} tuning by As or Ar implantation

In this Section, we investigate the As and Ar implantation technique for nMOSFETs. For this study we used nmos devices fabricated on p-type (001)/<100> silicon substrates. As a dielectric, 3.2 nm HfSiO (60% Hf) was deposited by MOCVD on a 1 nm in-situ steam generated (ISSG) SiO_2 interface layer. 2, 5, 10 or 15 nm PVD TiN was used as metal gate. In order to adjust the threshold voltage, As or Ar was implanted after the gate deposition with energies in the range from 2 to 8keV and implantation dose from 4×10^{15} to 6×10^{15} at/cm^2. Stopping and Range of Ions in Matter (SRIM) simulations place the implant primarily in the gate metal. A 5nm Si-cap was deposited on the TiN before implantation to prevent metal contamination in the implanter. No-implant devices with EOT in the range of 1.4 to 1.5nm and implant devices with EOT in the range of 1.35 to 1.4nm are processed. The transistors showed state of the art drive and off-current performance as shown in Fig. 1.

A. As gate implantation

Fig. 2 shows an example of the split CV curves for As implanted and no-implant reference devices with 15 nm TiN. The observed V_{th}/V_{fb}-reduction after As implantation shows an obvious dependence on the implant energy. However, no stretch out or any indication of device damage in the shape of CV curves is detected. Surprisingly, increase of the As implant dose (from 4×10^{15} to 6×10^{15} at/cm^2) reduces the V_{th}/V_{fb} shift. Singanamalla *et al.* [7] explained the implant induced V_{th}/V_{fb} shift based on the As ion pile-up at the metal/HK interface. Their reasoning is as follows: Arsenic is more electro-negative compared to Ti. This can lead to the formation of an interface dipole resulting in an Effective Work Function (EWF) reduction compared to no-implant reference devices. The Pauling electro-negativity values of As and Ti are known to be 2.18 and 1.62, respectively [13]. Due to the increased concentration of As at the metal electrode side of the Ti/high-k interface, As-Hf or As-O bonds are formed (in implanted devices) instead of Ti-Hf or Ti-O bonds (in reference devices). This results in a net magnitude increase of the interface dipole pointing from the dielectric to the metal electrode side causing an upward bending of the bands at the dielectric side and hence shifting the metal work function towards the Si conduction band-edge which in turn results in a shift (reduction) of V_{th}/V_{fb}. The band diagram in Fig. 3 drawn at flatband, shows how the formation of a dipole at the metal/high-k interface modulates the effective metal work function. Singanamalla *et al.* [3] also reported an additional reduction of the threshold voltage compared to the flatband voltage as a result of As reaching the Si channel. This is justified as Arsenic ions can give electrons to the p-type Si lattice and reduce the net hole concentration, hence acting as counter dopants. They expressed this as follows

$$V_{\text{th}} = V_{\text{fb}} + 2\phi_F + \frac{1}{C_{ox}}\sqrt{4\varepsilon_{si}qN_A\phi_F} - q\frac{D_I}{C_{ox}}. \quad (1)$$

D_I is the area concentration of counter-dopant species at the interface (cm^{-2}). In other words D_I is the dose of counter-dopants projected at the interface.

Additional V_{th}-reduction compared to V_{fb}-reduction due to the channel counterdoping is then expressed as

$$\Delta V_{\text{th}} = \Delta V_{\text{fb}} - q\frac{D_I}{C_{ox}}, \quad (2)$$

where ΔV_{fb} is the flatband voltage shift induced by the shift in the effective metal work function.

Fig. 4 shows inversion part of CV curves (obtained from split CV characteristics) of no-implant and As-implanted p-type devices with 10 nm TiN and high implant energy (8KeV). In agreement with the observations of Singanamalla *et al.* (discussed above), also our measured CV curves indicate Si channel counter doping. The shape of the CV curve is changed after implantation and stretch out is observed compared to the no-implant reference device. The presence of a partially inverted channel even at zero or negative gate bias is a clear evidence of the counter doping of the Si channel. The observed hump on the implanted CV curve indicates damage due to the implantation. As shown in Fig. 2, the effect of channel counter doping is negligible in implanted devices with 15 nm TiN even when implant energy of 8KeV is used. This suggests that as the TiN thickness is reduced, the maximum implant energy that can be used without distorting CV and IV curves due to excessive channel counter doping should also be reduced.

B. Ar gate implantation

In this section, we investigate the effect of gate implant of an inert species, i.e. Argon, on device threshold voltage. Fig. 5 summarizes the obtained V_{th}-reduction in As and Ar implanted devices with respect to a non-implanted reference device. Different implant energies and implant doses are included. Since Argon is inert, the observed ΔV_{th} on devices with Ar gate implant cannot be due to the channel counter doping. Also the dependence of V_{th} shift on implant energy is much stronger for As than for Ar implant which is another indication that channel counter doping plays a role only in the case of As implant. Remarkably, both As and Ar implant show less V_{th} shift with higher implant dose. As Argon is an inert element, it can also not modulate the metal work function. Consequently, the introduced model in Section II-A, relying on the formed dipole at the metal/high-k interface, is ruled out as a suitable explanation for the V_{th}-tuning mechanism when Ar is implanted. Moreover, Fig. 6 shows the V_{th} and V_{fb} reduction observed with inert Ar and As gate implant with respect to the no-implant reference device. We observe that the implant-induced shift is not identical for V_{fb} and V_{th}, and systematically, V_{fb} is less altered than V_{th}. As the data set is restricted to 15 nm TiN for As-implantation and due to the inert character of Ar, Si channel counter doping cannot explain the $\Delta V_{fb}/\Delta V_{th}$ gap.

In the following section, we further investigate the underlying mechanism of the implantation technique and propose a new model to explain the initial V_{th} and V_{fb}-control in nMOSFETs with HfSiO/TiN gate stack by trapped charge in HfSiO bulk defects.

III. Underlying mechanism of implantation-induced $\Delta V_{TH}/\Delta V_{FB}$

In this Section we further investigate the underlying mechanism of the implantation-induced voltage shifts.

A. Trap characterization of As or Ar-implanted devices

In order to investigate the effect of implantation on gate oxide trap density, we measure the energy profile of the initially present defects in the HfSiO gate oxide by Trap Spectroscopy by Charge Injection and Sensing (TSCIS) [14]. TSCIS relies on a controlled charging of defects by direct tunneling as a function of charging time (t_{charge}) and charging voltage (V_{charge}) [14]. This technique was developed to characterize traps in 10-20nm oxides targeted for flash interpoly dielectrics (IPD) or blocking dielectrics in charge trapping devices. We adapted the technique for thinner gate dielectrics by shortening t_{charge} as V_{charge} increases in order to make the scanning of 1nm SiO_2/3.2 nm HfSiO possible. The measured voltage-shifts vs. t_{charge} for increasing V_{charge}-V_{th} are shown in Figs. 7(a) and 7(b) for a 10 nm TiN no-implant reference device with $V_{th} = 0.86$V, and a 6keV, 4×10^{15} at/cm^2 As-implanted device with $V_{th} = 0.54$V, resp. By repeating V_{charge}-sweeps, it is verified that V_{charge} remains sufficiently low in order to avoid the creation of new traps. A self-consistent combination of the WKB-approximation for tunnelling and a Poisson solver, allows extraction of the energy profile of the HfSiO-traps with respect to HfSiO bottom of the Conduction Band (BCB) as shown in Fig. 8 for non-implanted and both Ar and As-implanted devices. Clear differences between the energy profiles of the initial traps in the implanted devices (having a low initial V_{th}) and the non-implanted reference devices (with high initial V_{th}) are observed [11]. In the non-implanted samples, the density increases for energy levels $>$0.8eV with respect to HfSiO BCB ('**deep**' traps), while for implanted devices no deep traps are observed and only '**shallow**' traps with energy level < 1 eV with respect to the HfSiO BCB are found. These results suggest the passivation of energetically deep traps after implantation. Since Argon is inert and has the same effect as As on the energy profile of the initial traps, we conclude that the electronic properties of As are not causing the deep trap density reduction. Possibly, only the implant energy is needed to change the trap density profile. We will investigate this subject further in Section V.

Inspired by the observations in Fig. 8, we characterize the defect profile of samples with different V_{th} adjustment process conditions and investigate whether the change in trap density profile is correlated with the device V_{th}.

B. Systematic correlation between V_{th} and density of deep traps

In order to quickly access the density of deep traps, we measured the voltage shift at the lowest V_{charge}=$V_{th}+\Delta V$ (with $\Delta V\approx$0.1V) after t_{charge}=1000 s. This shift is proportional to the density of traps that can be scanned between 0V (= fresh device) and $V_{th} + \Delta V$, corresponding to HfSiO energy levels in the range $\sim$1.2-1.5eV below HfSiO BCB. We will refer to this voltage-shift as $V_{th,deep}$ (as defined also in Fig. 7(b)). As shown in Fig. 9, $V_{th,deep}$ measured in samples with different TiN thickness, with As or Ar implantation and with various implant energies and doses are all systematically correlated with their corresponding V_{th}-values. The indicated points 1 and 2 in Fig. 9 correspond to non-implanted and the 6 keV, 4×10^{15} at/cm^2 As-implanted samples, respectively, discussed in Fig. 7 and 8.

To emphasize the fundamental nature of the correlation in Fig. 9, we lift out one specific case indicated with arrows in Fig. 9. When the As implant dose is increased from 4×10^{15} at/cm^2 with corresponding V_{th} =0.64 V, to 6×10^{15} at/cm^2, V_{th} surprisingly increases to 0.86V. In other words, a too high As implant dose annihilates the V_{th} adjust. Also for this case, the deep trap density is high and close to the non-implanted case corresponding to less passivated deep traps.

Based on the revealed correlation in Fig. 9, we propose that the density of energetically deep electron traps in the HfSiO modifies the V_{th} and the density of these traps can be controlled by changing energy and dose of the As/Ar implant. Also the thickness of the metal gate influences the effect of the implant.

In samples without implantation (with high initial V_{th}), the energy profile shown in Fig. 8 suggests that the measured traps are merely a low energy tail (energy $<\sim 1.5$eV) of a broader defect distribution and correspond to only a few mV voltage-shift (as shown in Fig. 7(a)). As schematically presented by the dashed line in Fig. 8, we propose that this distribution continues to energy levels below the metal work function level, where the majority of the traps (with energy levels $>\sim$ 1.5eV below HfSiO BCB) are negatively charged by electron injection from the gate, hence causing their high initial V_{th}/V_{fb}. We suggest that implant removes the main part of the distribution, resulting in a reduction of the negative charge in the dielectric and therefore reduces-V_{th}/V_{fb} as schematically shown in Fig. 10.

IV. Proof of the model

In previous section, we proposed that not a surface dipole, but uniformly distributed high-k defects determine V_{th} and V_{fb}. To unambiguously prove this hypothesis, the main part of the defect distribution in HfSiO, i.e. the part below the metal work function, needs to be experimentally characterized and the measured trap density should correspond to the V_{th}/V_{fb}-shift observed when removing these traps.
To obtain this goal, dedicated charging/discharging experiments were carried out on a special set of structures. These will be discussed in this Section.

A. HfSiO charging/discharging experiments

The devices used in this section are nMOSFETs with either 2-layer or 3-layer gate dielectric stacks. The 2-layer dielectric stacks have 3.2, 5 and 7 nm HfSiO dielectric (60% Hf), deposited by MOCVD on a 1 nm In-situ steam generated (ISSG) SiO_2 interface layer. 10 nm PVD TiN was used as metal gate. A work function of $\sim$4.5eV is adopted in this Section [15]. In order to adjust the threshold voltage, Ar

was implanted through the gate with energy of 4keV with implantation dose of 4×10^{15} at/cm^2. The 3-layer stacks have 1 nm SiO_2, 3.2 nm HfSiO and an additional 5 nm HTO (High Temperature Oxidation) SiO_2 layer. Table I summarizes the samples.

We first investigate voltage shifts in the three-layer stack (S5). The presence of a 5 nm SiO_2 between the high-k and the metal gate prevents HfSiO bulk defects to be charged from the metal gate. If the HfSiO defect energy level is below the Si-valence band, charging can still occur from the substrate since the tunnel barrier is only $\sim$1nm. However, we will now demonstrate that the HfSiO in the fresh device is uncharged. To achieve this, we apply a negative gate bias in order to discharge initially charged defects in the HfSiO to the substrate, as shown in Fig. 11(a). This is comparable to an erase operation in a charge-trap memory (like TANOS), but because of the ultra-thin tunnel barrier, voltage shifts need to be measured by a fast sensing technique (we use $\sim$3ms sensing at V_{sense}) identical to the one developed for minimized-relaxation-NBTI [16] or TSCIS [14]. As shown in Fig. 11(c), negative gate bias results in zero voltage shift, indicating no electron discharging to the substrate is possible, neither any hole trapping is observed down to V_g = -3.2 V.
The low initial V_{fb} = -0.8V in combination with this zero constant voltage shift confirms the absence of initially charged traps in HfSiO. This also proves that there is no significant electron defect density with energy levels below the Si valence band as they will discharge immediately via the interface states when negative voltage is applied. The high-k is therefore neutral in a fresh device.
By applying a positive gate bias (Fig. 11(b)), comparable to a write operation in memory terminology, a huge positive voltage shift is observed, as shown in Fig. 11(c). This confirms that uncharged defects in HfSiO can trap electrons injected from the inversion layer in the Si conduction band. The constant voltage shift at the highest V_g = 6.5V as a function of t_{charge} points out that the defect band is completely charged. If a uniformly distributed trap density in HfSiO is assumed, a trap volume density of $\sim 3.8\times10^{19}\,\mathrm{cm}^{-3}$ corresponds to the observed voltage-shift of $\sim$ 3V in Fig. 11(c).

The trapped electrons are very easily discharged again, since applying V_g = -0.5V for 10s is already sufficient to remove $\sim$80% of the charge. This suggests that the HfSiO defects are energetically located directly opposite to the Si band gap, i.e. at $\sim$1.5-2.5eV below the HfSiO BCB, as they can tunnel back easily to the substrate at low negative bias through Si/SiO_2 interface states. The observed trap energy level agrees with the *ab-initio* calculated energy levels of the most important defects in HfSiO i.e. oxygen vacancies [17].

B. V_{fb} -tuning by HfSiO charged defects

Assuming that the trap volume density found in the previous 3-layer experiment remains present in a 2-layer stack (S1), the V_{fb} is calculated to be -0.39V, while the actual measured V_{fb} is -0.44V. A match between measured and calculated V_{fb} is achieved when the charged trap density is reduced to $2.6\times10^{19}\,\mathrm{cm}^{-3}$, which is still in the same order of magnitude. We conclude that in 2-layer stack (S1), electrons from the metal gate do not entirely fill all available trap centres, possibly because part of them are either located above the metal Fermi level, or are too far from the metal/dielectric interface to be accessed from the metal gate. The alternative explanation that the trap density is reduced because of the processing differences between samples S1 and S5 can, however, also not be excluded.

The charged defects are schematically drawn in Fig. 12(a). At flatband condition, the charge density cannot be uniform as function of position because: i) charge-induced band bending shifts the energy profile of defects upwards with respect to the metal gate and ii) Filling of the defect band is determined by the detailed balance between metal fermi level and the energy position of defects.
As we have not brought the defect energy profile into account, the density of $2.6\times10^{19}\,\mathrm{cm}^{-3}$ is an average number.

If all traps are removed, the calculated V_{fb} reduces to -0.546V, matching the measured V_{fb} on sample S2 which was treated with an Ar implant. The V_{fb} -shift between samples S1 and S2 is $\sim$100mV, while the V_{th} -shift is $\sim$220mV. With the physical picture presented in this Chapter, this difference can be explained by extra charge injection at V_{th} from the inversion layer to neutral (empty) traps near the SiO_2/high-k interface.

To determine how far the charging from the metal gate reaches at flatband condition, 2-layer stacks with 1nm SiO_2 and increasing high-k thickness (S1, S3 and S4) are investigated. Since the V_{fb} is constant (-0.44V) with EOT-increase, we conclude that the same profile of charged defects ($\sim$ maximum 3.2nm wide) is located at the gate side as shown in Fig. 12. This is understood based on the equation of V_{fb} written as

$$V_{\mathrm{fb}} = \phi_{\mathrm{ms}} - \frac{1}{\varepsilon_0}\left[\int_0^d \frac{x\rho(x)}{\varepsilon_r}\,dx + \int_d^{t_{ox}} \frac{x\rho(x)}{\varepsilon_r}\,dx\right], \qquad (3)$$

with ϕ_{ms} the difference between the work function of metal and Si, $x = 0$ is in the interface at the metal side and $d \sim$ 3.2nm. A constant V_{fb} with increased EOT is obtained only when the second integral in this equation is equal to zero. As the first integral is the same for all three stacks, same V_{fb} is obtained.

Since a constant V_{fb} versus EOT is observed, one could assume the presence of a dipole at the dielectric/gate interface, as suggested in also literature [3, 8]. However, we showed that the flatband shift is due to the change of high-k bulk charge, rather than to the modulation of the metal work function at the interface only. As also mentioned in Section II, the difference between both interpretations becomes clear when the gap between implantation-induced V_{fb} -shift (100mV) and V_{th} -shift (220mV) is considered. A dipole without assuming additional counter doping effects in the substrate [3] cannot explain the $\Delta V_{fb}/\Delta V_{th}$ gap. In our samples, counter doping effects are, however, excluded since Ar is an inert element. This rules out the dipole model as a suitable explanation for the V_{th}/V_{fb} -tuning mechanism with high-k/metal gates.

Since the high-k defects cannot be charged further than

$\sim$3.2nm away from the metal gate interface, the defects in 5 and 7nm HfSiO (samples S3 and S4) are still uncharged close to the substrate interface. It is expected that these defects can still be charged by the electron injection from the substrate as illustrated in Fig. 13(a). Indeed, a Voltage-shift of up to 0.35V, shown in Fig. 13(b), confirms our expectation. Also the observed voltage shifts occurring at $t_{charge} < 0.01$s indicate that the trapping is mostly close to the substrate interface.

V. Physical mechanism of implantation-induced V_{TH} /V_{FB} -tuning

As was shown in Fig. 8, gate implantation of an inert species such as Ar results in the same effect as As implantation on the energy profile of the initially present traps in HfSiO. Therefore in section III, we concluded that the electronic properties of As were not causing the deep trap density reduction and only the implant energy was needed to change the trap density profile.

In order to present a physical explanation for the implantation effect on V_{th} and V_{fb}, physical analysis of the implanted devices [18] is combined with the electrical results presented in previous section. Atom Probe (AP), a nano-scale characterization technique [19], provides a chemical composition and a 3D reconstruction of the gate stack.

Fig. 14 shows atom profile with and without As implantation in the gate. Nitrogen (N) is tracked by N^{2+}. This state of charge is present in the high-k dielectric and at the interface for the implanted samples only and is below the measurement sensitivity for the non-implanted samples. Signals of other elements such as Si, Hf, etc. are the same in both implanted and non-implanted devices. This indicates that some nitrogen atoms are not in their standard chemical environment compared to the non-implanted sample. Based on these results, we speculate about the role of Nitrogen (N) for the implanted samples as follows: the V_{th}/V_{fb} modulation is explained by passivation of HfSiO bulk defects due to the release of nitrogen from the gate metal during implantation. According to the *ab-initio* calculations of Xiong and Robertson [20], the nitrogen-passivated defects are shifted to energetically shallower levels in agreement with our earlier observations in Fig. 8. However, the possibility that the shallow traps are induced by implantation damage cannot be excluded.

VI. Interpretation of the reliability results

In this Section, we focus on the impact of As and Ar implantation on the reliability of V_{th} -adjusted transistors and interpret the results of the reliability tests based on the defect profiles characterized in Section III.

PBTI was measured on $W \times L = 10 \times 1\,\mathrm{cm}^2$ MOSFETs at 125°C. Lifetime was determined at 30mV V_{th} -shift. Different stress voltages in the range 1.38 to 1.96V and different sense voltages in the range 0.34 to 0.62V were used. The V_{th} kinetics during PBTI stress follow a power-law time dependence and as shown in Fig. 15, the implanted samples have a larger V_g acceleration factor compared to no-implant samples. Consequently, PBTI lifetime is considerably improved with As or Ar implantation.

In our recent work [21], we made the link between the PBTI results and the defect profiles characterized by TSCIS shown in Fig. 8 and we explained that the TSCIS methodology (performed at room temperature) is very similar to fast V_{th} -evaluation methods developed for minimizing the relaxation during PBTI measurements [16]. In fact, TSCIS could be described as a PBTI measurement at room temperature.

In Fig. 16(a) and (b), a cross section of the V_{th} -shifts vs. t_{charge} data (from TSCIS) at a fixed threshold voltage shift is taken. The corresponding charging times are displayed vs V_g-V_{th} as shown in Fig. 16(c). It is clear that voltage shifts due to shallow traps in devices with implantation (observable in the corresponding energy profile shown in the inset of the figure) result in a steeper charging time extrapolation curve compared to deep traps in non-implanted reference devices, which is consistent with the steeper PBTI lifetime curves shown in Fig. 15. This proves that PBTI is directly correlated to the energy profile of initially present defects.

Electron trap filling is the main underlying mechanism in PBTI [22]. As or Ar-implanted devices contain shallow traps (discussed in Section III and shown in Fig. 8) which are only accessible at high gate voltages. At lower voltages, filling of these shallow traps does not occur, hence resulting in higher PBTI lifetimes and steeper voltage acceleration.

In order to study the defect generation, Constant Voltage Stress (CVS) is applied on an $L = 1\mu$m and $W = 1\mu$m transistors. Much higher stress voltages are used compared to PBTI. The breakdown (BD) is triggered with a current step of 500nA and a reliability spec of 0.01% failures after 10 years on 0.1 cm^2 effective area is used for the lifetime extrapolation. While PBTI results mainly from the filling of existing traps, TDDB studies the effect of generated defects. Fig. 17 shows different voltage dependences of the trap generation in non-implanted and implanted devices. This indicates different kinds of generated defects in these devices.
This conjecture is confirmed by TSCIS characterizing different defect energy profiles in the stressed devices as shown in Fig. 18. The energy profile of the generated defects also differs from the initially present defects shown in the bottom of the same figure. For the As-implanted devices, a reduction of defect density in the shallow energy range is observed after stress. We speculate that passivation of defects (similar to the passivation after gate-implantation) has occurred due to stress. For lifetime extrapolation to operating conditions, the difference in voltage dependence (different power law exponents in Fig. 17) is compensated by the difference in β (= a measure for the number of traps participating in breakdown path) resulting in nearly identical lifetime for both devices.

VII. Summary

In this paper V_{th} /V_{fb} tuning of nMOSFETs with HfSiO/TiN gate stacks obtained by As or Ar gate implantation was studied.
To advance our understanding of the underlying mechanism of the implantation-induced V_{th} and V_{fb} shifts, we reviewed a dipole model from literature suggesting that As ions implanted through the gate result in a shift in the metal work function.

However, we pointed out the insufficiency of this model to explain the obtained voltage shifts when an inert element such as Ar is implanted.

To develop an alternative model, we studied the impact of V_{th}/V_{fb} -adjustment in nMOSFETs by measuring the trap density in the gate dielectric using TSCIS. We found that energetically deep traps in no-implant devices are passivated after gate implantation, possibly by the released N from the gate. We detected additionally shallow traps in the V_{th} -adjusted devices which are either i) the passivated defects energetically shifted upwards or ii) newly generated defects due to the implant damage.

We revealed a fundamental correlation between the energetically deep trap density and the initial V_{th} independent of the V_{th} -adjustment process (gate implants or gate thickness variation). Therefore, we proposed that the initial V_{th}/V_{fb} in nMOSFETs with HfSiO/TiN gate stack is controlled by trapped charge in HfSiO bulk defects.

We experimentally proved this model by completely charging and discharging the HfSiO defects and quantifying the effect on the V_{th}/V_{fb} . We found that due to the position of the metal WF, electrons occupy the HfSiO defects in the proximity of the gate in fresh devices causing a high initial V_{th}/V_{fb} -value. We concluded that V_{th}/V_{fb} -adjustment by As or Ar implantation is due to the reduction of charged trap density in the HfSiO.

In the final part of the paper, we investigated the reliability of the implanted nMOS transistors with 10nm TiN. We showed that, as PBTI is determined by filling of the existing traps, the PBTI lifetime is mainly dominated by the energy profile of initially present defects. As the shallow traps in implanted devices are not accessible at low voltages, PBTI lifetime is considerably improved at real operating conditions. On the other hand, TDDB is determined by generated defects which have different energy profile compared to the initially present defects.

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TABLE I
SUMMARY OF THE SPECIALLY DESIGNED STACKS STUDIED IN THIS SECTION WITH THEIR CORRESPONDING EOT, INITIAL V_{TH} AND V_{FB}.

		Implant	EOT	V_{fb}	V_{th}
S1	1nm SiO_2/ 3.2 nm HfSiO	-	1.53 nm	-0.44	0.82
S2	1nm SiO_2/ 3.2 nm HfSiO	Ar	1.46 nm	-0.54	0.60
S3	1nm SiO_2/ 5 nm HfSiO	-	1.71 nm	-0.44	0.85
S4	1nm SiO_2/ 7 nm HfSiO	-	2.21 nm	-0.44	0.88
S5	1nm SiO_2/ 3.2 nm HfSiO /5 nm SiO_2	-	5.08 nm	-0.80	0.82

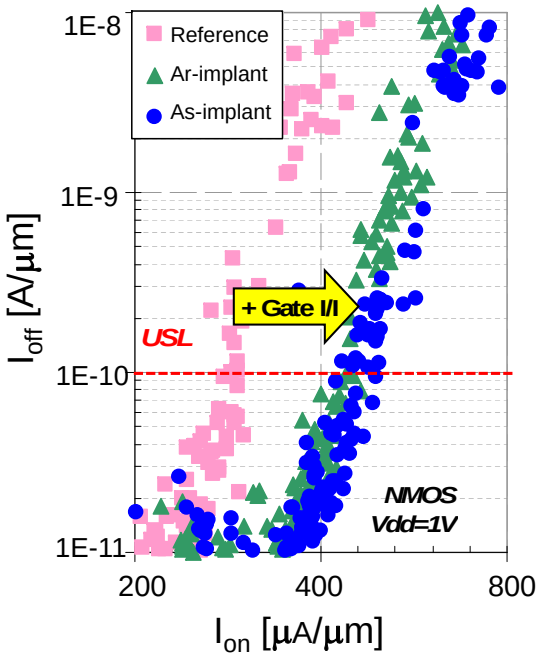


Fig. 1. NMOS I_{on} vs. I_{off} for no-implant reference and As and Ar gate implanted devices with 10nm TiN. Both implanted devices show considerable improvement in drive current compared to no-implant device.

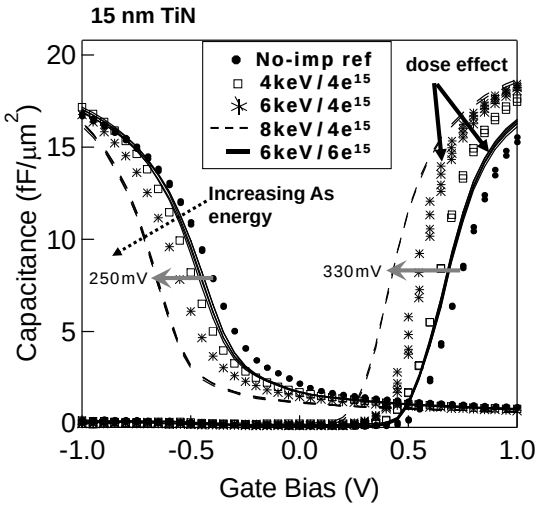


Fig. 2. The split CV characteristics measured on p-type devices from TiN/HfSiO/SiO_2 gate stacks with and without As implantation. As was implanted through the gate at energies in the range 4 to 8keV with implantation dose from 4×10^{15} to 6×10^{15} at/cm^2. All gate stacks have 15 nm TiN.

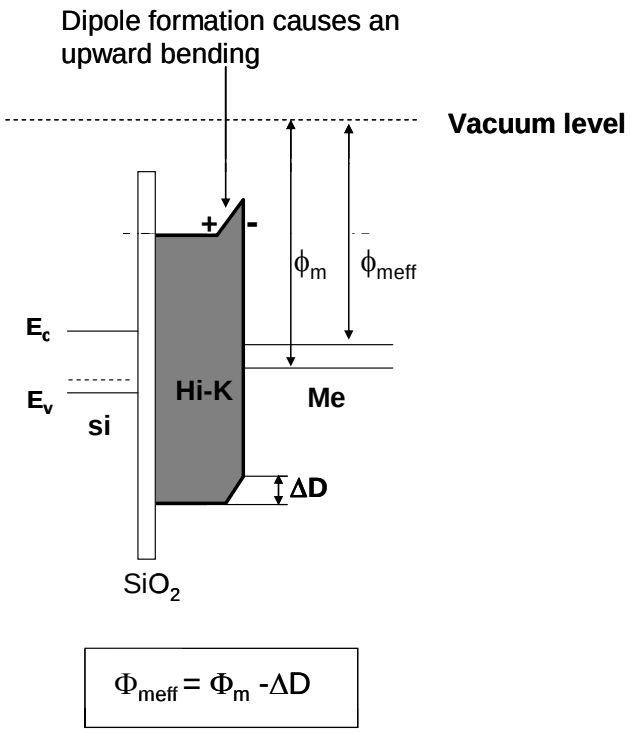


Fig. 3. The band diagram drawn at flatband shows upward bending of the bands at the dielectric side because of the formation of a dipole at the metal/high-k interface. As a consequence of this upward bending, the effective metal work function is modulated (after Singanamalla [3, 7]).

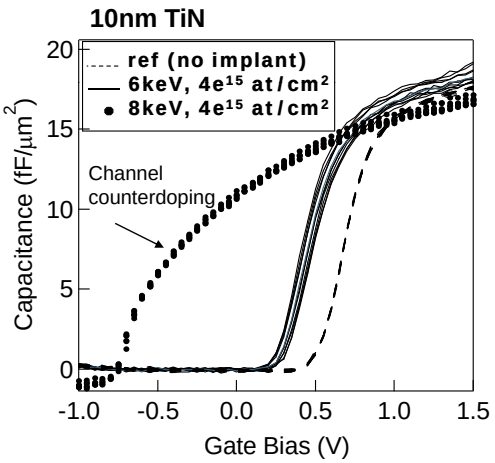


Fig. 4. Inversion part of CV characteristics (obtained from split CV measurements) of p-type devices from TiN/HfSiO/SiO_2 gate stacks with and without As implantation. All gate stacks have 10 nm TiN. Partially inverted channel even at negative gate bias indicates channel counterdoping when too high implant energy is used.

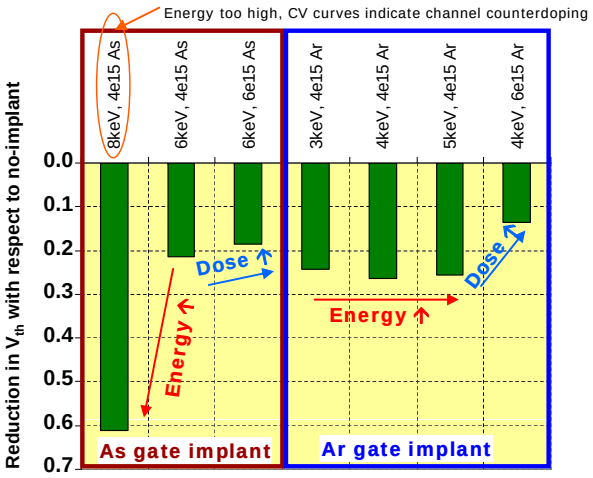


Fig. 5. V_{th} reduction of As and Ar implanted devices with respect to no-implant reference device. Different implant energies and implant doses are included. All gate stacks have 10 nm TiN.

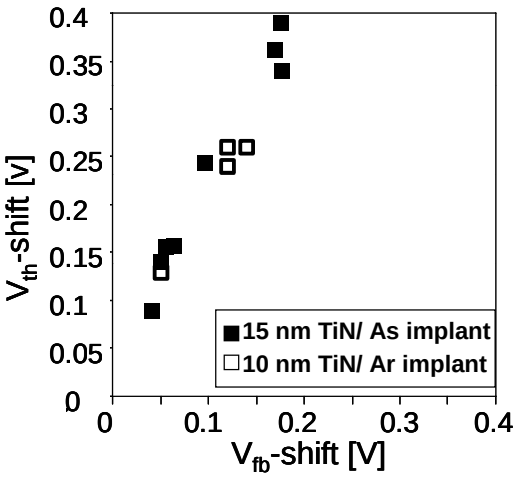


Fig. 6. V_{th} and V_{fb} reduction observed with Ar/As gate implant with respect to no-implant reference device. Implantation affects the V_{th} much more than V_{fb}. In order to limit the effect of channel counterdoping, the data set is restricted to 15 nm TiN for As-implantation.

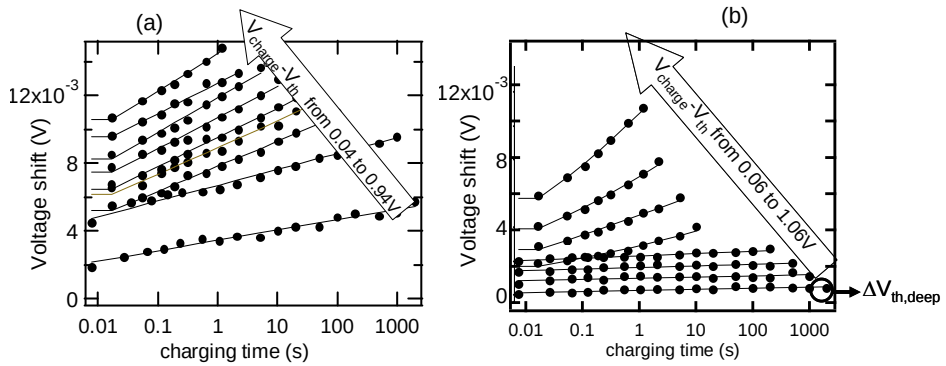


Fig. 7. (a) Voltage-shifts as a function of t_{charge} for increasing V_{charge}-V_{th} on 10 nm TiN non-implanted reference (E_{field}= (V_{charge}-V_{th})/EOT= 0.26 to 6.18MV/cm) and (b) 10 nm TiN As-implanted devices (E_{field}= 0.43 to 7.6MV/cm). Significant differences are readily observed and translated into distinctly different energy profiles shown in Fig. 8. The voltage-shift after 1000s at the lowest V_{charge} can serve as a quick measure for the density of the energetically deepest traps.

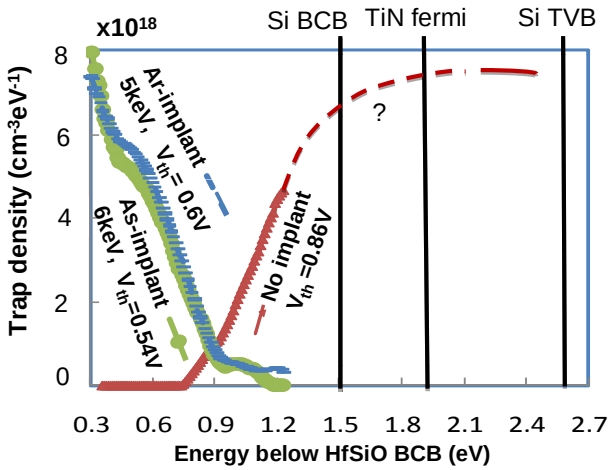
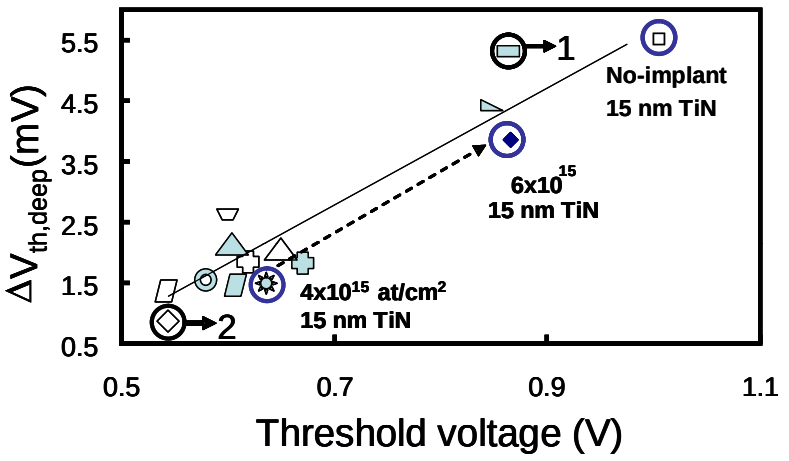


Fig. 8. The energy profile of the HfSiO trap density as extracted from the data in Fig. 7. The energy scale is calculated from the bottom of the conduction band (BCB) in high-k, assuming a 1.5eV offset to the Si BCB. For reference devices, the density increases for energy levels >0.8eV ('deep' traps), while for As-implanted devices only 'shallow' traps with energy level < 1 eV are observed. Ar implantation has the same effect as As-implantation. The dashed line indicates the possible extension of the trap density for reference samples to deeper energy levels. This is discussed in Section IV.



		TiN thickness(nm)	implant energy(keV)	implant dose(at/cm^2)
▱	As	5	2	4.00E+15
▱	As	5	4	4.00E+15
✚	Ar	10	3	4.00E+15
△	Ar	10	5	4.00E+15
▽	Ar	10	4	4.00E+15
△	As	10	6	4.00E+15
▭	-	10	none	none
◇	As	10	6	4.00E+15
◺	-	10	none	none
◎	-	2	none	none
✚	-	5	none	none
✸	As	15	6	4.00E+15
□	-	15	none	none
◆	As	15	6	6.00E+15

Fig. 9. The correlation between the density of the deep traps quantified by $V_{th,deep}$ and the initial V_{th}. The plot includes 2, 5, 10 and 15 nm TiN thickness, Ar and As implants with implant energy between 2keV and 6keV and dose from 4×10^{15} at/cm^2 to 6×10^{15} at/cm^2. The indicated points 1 and 2 correspond to non-implanted and As implanted devices, respectively, shown in Figs. 7 and 8. When the implant dose is increased from 4×10^{15} at/cm^2 to 6×10^{15} at/cm^2, both the V_{th}-adjust and the passivation of deep HfSiO traps are undone.

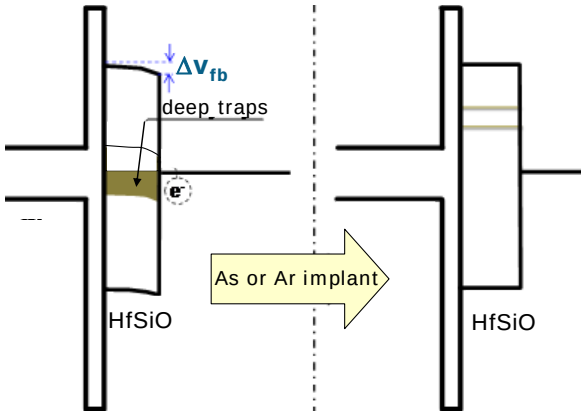


Fig. 10. Band plot at flatband voltage of a 1nm SiO_2/3.2nm HfSiO shows how the charged traps in the bulk of HfSiO control the V_{th}/V_{fb}. Due to As or Ar implantation, deep defects are passivated causing a reduction of V_{th}/V_{fb}. Energetically shallow traps appear after implantation (indicated as a defect band in the right-hand side figure), but remain uncharged and have therefore no impact on the V_{th}/V_{fb}.

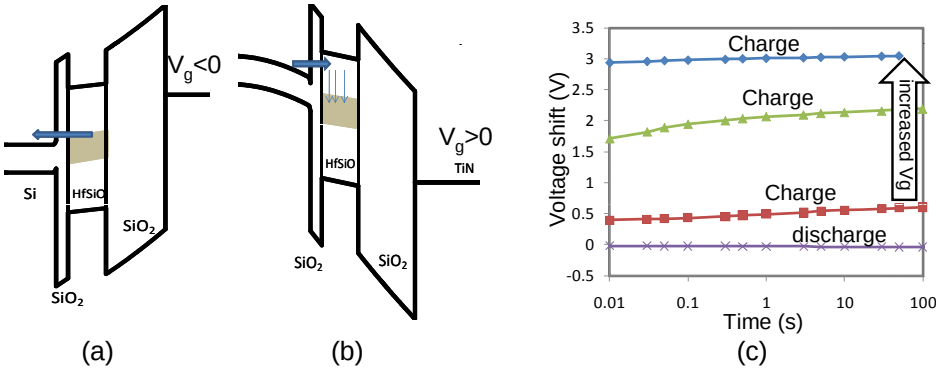


Fig. 11. Discharging (a) and charging (b) of stack S5 result in voltage-shifts presented in (c). No voltage-shift is observed after discharging as the defects are uncharged. Consistently, charging of the defects results in a pronounced voltage-shift that saturates at $\sim$ 3V shift.

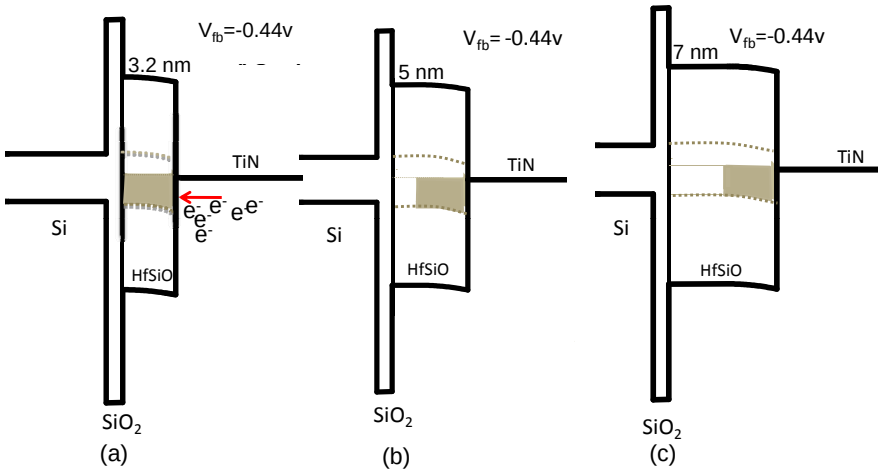


Fig. 12. Observing the same V_{fb} while the HfSiO thickness is increased from 3.2 (a) to 5 (b) and 7 nm (c) suggests that the same defect profile is located in the proximity of the gate electrode.

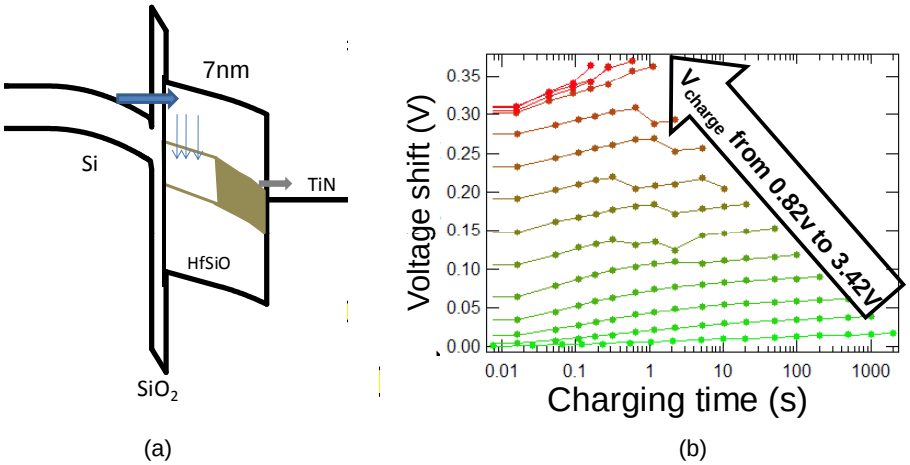


Fig. 13. The uncharged part of the defect band in stack S4 with 7nm HfSiO can be charged by electrons injected from the substrate (a) causing voltage shifts as a function of t_{charge} for increasing V_{charge} (b).

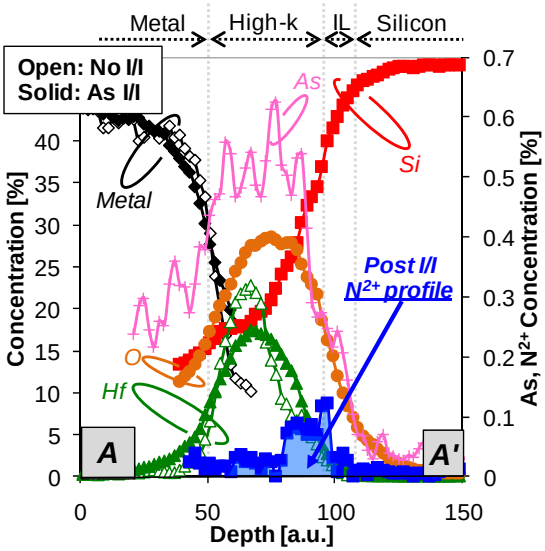


Fig. 14. Chemical profile measured by Atom probe with and without gate implantation indicates the release of the Nitrogen atoms from the gate and their diffusion into the stack. Nitrogen (N) is present in the high-k dielectric and at the interface for the implanted samples only. Signals of other elements are the same in both implanted and non-implanted devices. Open symbols for Si and O are not included for clarity of the picture.

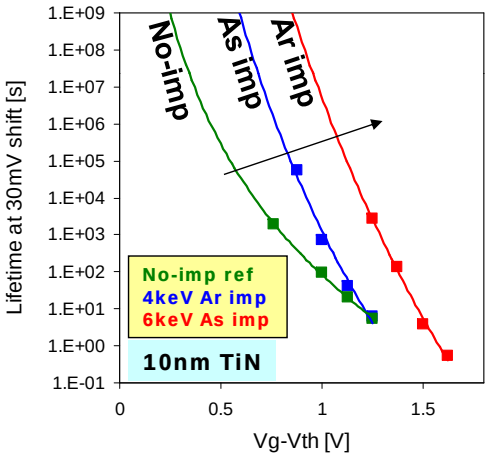


Fig. 15. PBTI lifetime as a function of V_g-V_{th} for no-implant and implanted devices. PBTI lifetime is considerably increased with implants. This is mainly due to the steeper V_g-acceleration for implanted devices.

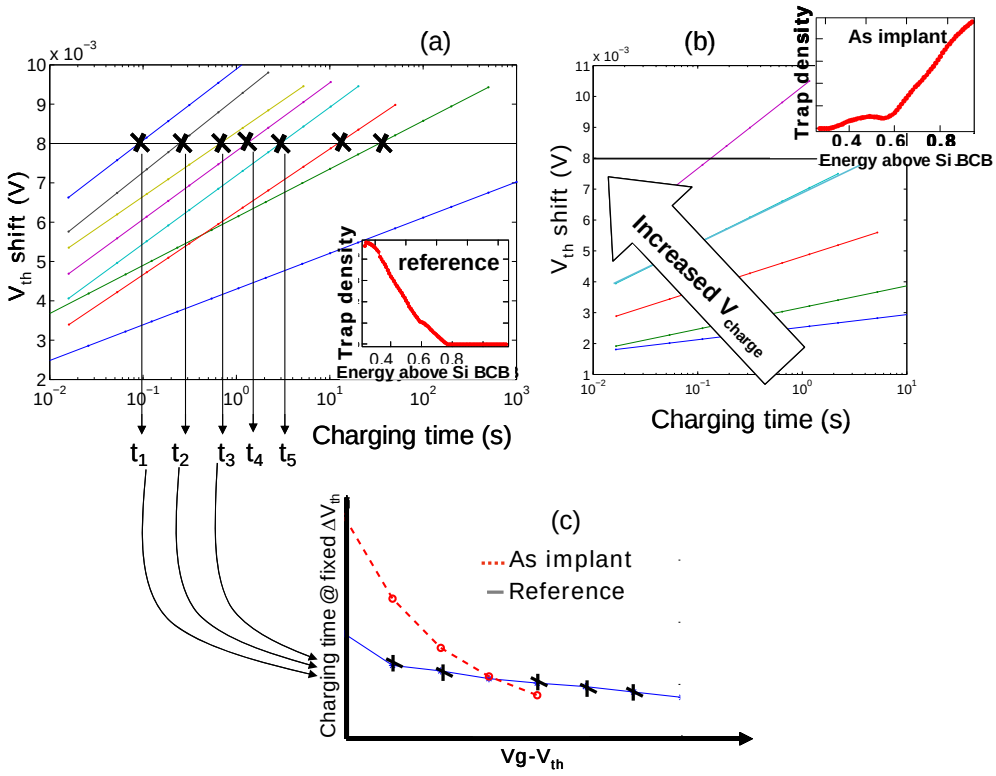


Fig. 16. (a) and (b) Cross section of the V_{th} shifts vs. t_{charge} for increasing V_{charge} (resulted from TSCIS) at a fixed threshold is taken. (c) The corresponding charging times are displayed vs. V_g-V_{th}. Energetically shallow defects in devices with implant (observable in the energy profile shown in the inset) result in a steeper charging time extrapolation curve. As TSCIS measurements are performed at 25°C, a lower threshold (compared to 30mV for PBTI) is chosen.

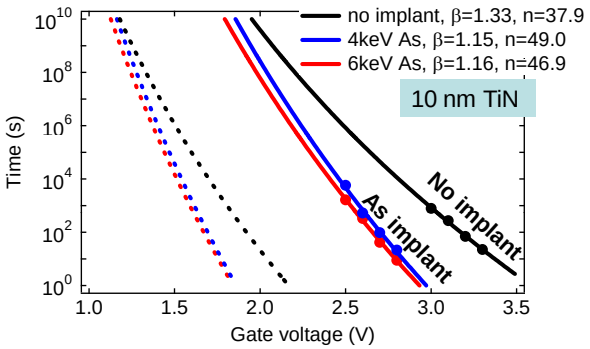


Fig. 17. Lifetime extrapolation for As-implanted and non-implanted reference devices. The trap generation in non-implanted and implanted devices show different voltage dependences. However, same lifetime within spec is predicted for all samples. The dashed lines indicate the extrapolation to operating conditions.

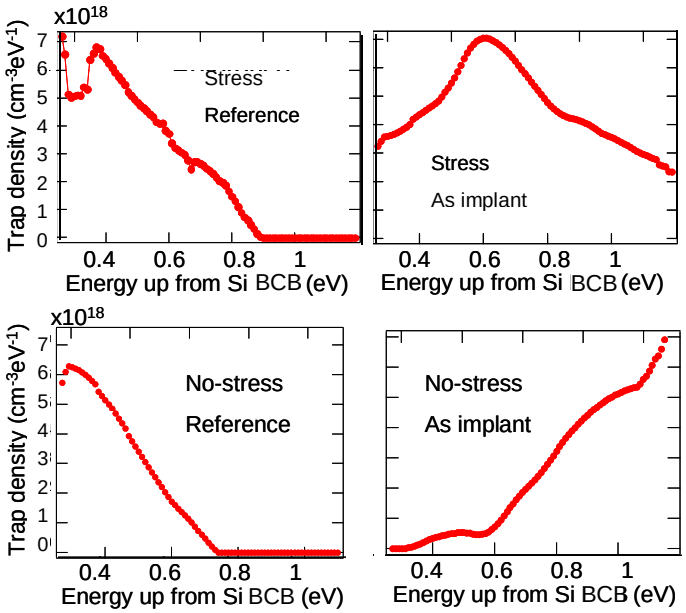


Fig. 18. (Top) Defect profiles of the stressed non-implanted and implanted devices characterized by TSCIS. Generated defects with Constant Voltage Stress are different in non-implanted and implanted devices. Also, these profiles differ from the profiles of the initially present defects (bottom).