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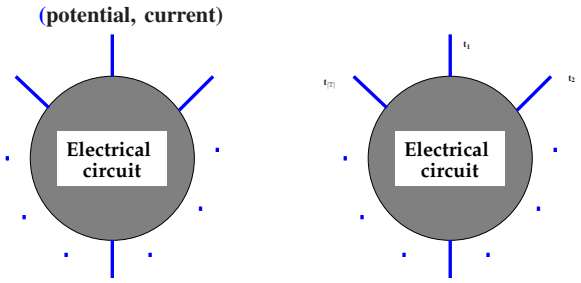
The Behavior of Resistive Circuits

Jan C. Willems and Erik I. Verriest

***Abstract*— We apply the modeling methodology of tearing, zooming, and linking to passive linear resistive circuits. The purpose of the article is to present necessary and sufficient conditions that govern the terminal voltage/current behavior of such a circuit. In its simplest form, these conditions require the matrix that relates the voltage vector to the current vector to be symmetric hyperdominant with zero excess. We also discuss the decomposition of a resistive circuit into a set of indecomposable components.**

I. The terminal behavior

We view an electrical circuit as a device that interacts with its environment through a finite number of wires (henceforth called *terminals* and denoted by $t_1, t_2, \ldots, t_{|\mathbb{T}|}$), as illustrated in the figure below. Associated with each terminal, there is a



potential and a *current* (by convention counted positive when it runs into the circuit). Even though only potential differences are physically measurable, we consider the terminal potentials and the currents as the essential quantities which describe how a circuit interacts with its surroundings.

Assuming that potentials and currents are expressed in some units (say, volts and amps), we obtain that the instantaneous interaction of the circuit with its surroundings is specified by a vector $(V,I) \in \mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|}$. In this paper we restrict attention to memoryless circuits. Hence only the instantaneous behavior matters. The set of pairs $(V,I) \in \mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|}$ that are compatible with the internal structure of the circuit and resistor values forms a subset $\mathscr{B} \subseteq \mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|}$, called the *terminal behavior* of the circuit. $(V,I) \in \mathscr{B}$ means that the circuit allows the vectors (V,I) of terminal variables, while $(V,I) \notin \mathscr{B}$ means that the circuit forbids the vectors (V,I) of terminal variables. In this paper, we study which subsets $\mathscr{B} \subseteq \mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|}$ can occur as the terminal voltage/current behavior of an interconnection of a finite set of linear nonnegative resistors.

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We now explain briefly some notions from graph theory that are needed in the remainder of the paper. A *graph with leaves* $\mathscr{G}$ is defined as

$$\mathscr{G} = (\mathbb{V}, \mathbb{E}, \mathbb{L}, f_{\mathbb{E}}, f_{\mathbb{L}})$$

with $\mathbb{V}$ the set of *vertices*, $\mathbb{E}$ the set of *edges*, $\mathbb{L}$ the set of *leaves*, $f_{\mathbb{E}}$ the *edge incidence map*; $f_{\mathbb{E}}$ maps each element $e \in \mathbb{E}$ into an unordered pair $[v_1, v_2]$, with $v_1, v_2 \in \mathbb{V}$, and $f_{\mathbb{L}}$ the *leaf incidence map*; $f_{\mathbb{L}}$ is map from $\mathbb{L}$ to $\mathbb{V}$.

If $f_{\mathbb{E}}(e) = [v_1, v_2]$, then we call v_1 and v_2 *incident* to $e \in \mathbb{E}$, and if $f_{\mathbb{L}}(e) = v$, then we call v *incident* to $e \in \mathbb{E}$. A graph with leaves is thus basically an undirected graph in which some 'edges', called 'leaves', are adjacent to only one vertex. Note that we denote by $[a,b]$ an unordered pair. By definition, therefore, $[a,b] = [b,a]$, and $a = b$ is possible. Contrast this with the notation for an ordered pair (a,b) which is unequal to (b,a) unless $a = b$, and with the set notation $\{a,b\}$ which is equal to $\{b,a\}$, and hence unordered, but not suitable for our purpose, since $\{a,a\} = \{a\}$.

The *degree* is a map from $\mathbb{V}$ to $\{0,1,2,\cdots\}$ such that $d(v)$ is equal to the number of edges plus leaves that are adjacent to v. A *self-loop*, that is an edge $e \in \mathbb{E}$ with $f_{\mathbb{E}} = [v,v]$, counts for 2 in the degree.

In a *digraph with leaves* each edge and leaf have a direction. In particular, the edge adjacency map $f_{\mathbb{E}}$ is then a pair of maps $f_{\mathbb{E}}^{\text{source}}, f_{\mathbb{E}}^{\text{sink}}$, meaning that the direction of the edge $e \in \mathbb{E}$ runs from $f_{\mathbb{E}}^{\text{source}}(e)$ to $f_{\mathbb{E}}^{\text{sink}}(e)$.

II. Linear resistive circuits

A linear resistive circuit is defined by a *circuit architecture*, which is a graph with leaves $\mathscr{G} = (\mathbb{V}, \mathbb{E}, \mathbb{T}, f_{\mathbb{E}}, f_{\mathbb{T}})$ and a *resistance map* $\rho : \mathbb{E} \to [0,\infty)$. Denote by $d : \mathbb{V} \to \mathbb{N}$ the degree.

The idea underlying this definition is as follows. The leaves, the elements of $\mathbb{T}$, correspond to the external terminals through which the circuit interacts with its environment. The edges, the elements of $\mathbb{E}$, correspond to resistors, with $\rho(e)$ the value of the resistor (say in ohms) in edge $e \in \mathbb{E}$. The vertices, the elements of $\mathbb{V}$, serve as connectors. If the degree of $v \in \mathbb{V}$ is $d(v)$, then v connects $d(v)$ wires, some of which originate from the resistors (corresponding to the edges incident to v) and some of which originate from the external terminals (corresponding to the leaves incident to v).

III. Behavioral equations of a resistive circuit

There are a number of ways to arrive at equations for the terminal behavior of a linear resistive circuit. The classical way of introducing as auxiliary variables the vertex potentials

and the edge currents is convenient. Label the vertices as $v_1, v_2, \ldots, v_{|\mathbb{V}|}$, the edges as $e_1, e_2, \ldots, e_{|\mathbb{E}|}$, and the leaves (which correspond to the external terminals) as $t_1, t_2, \ldots, t_{|\mathbb{T}|}$. Assign a direction to each edge. Now introduce the *edge incidence matrix* $\mathscr{I}_{\mathbb{E}} \in \{1,-1,0\}^{|\mathbb{V}|\times|\mathbb{E}|}$ and the *leaf incidence matrix* $\mathscr{I}_{\mathbb{T}} \in \{1,0\}^{|\mathbb{V}|\times|\mathbb{T}|}$ by

$$(\mathscr{I}_{\mathbb{E}})_{i,j} = \begin{cases} 1 & \text{if } e_j \text{ is not a self-loop incident to and directed towards } v_j, \\ -1 & \text{if } e_i \text{ is not a self-loop incident to and directed away from } v_i, \\ 0 & \text{if } e_i \text{ is not incident to } v_j, \end{cases}$$

$$(\mathscr{I}_{\mathbb{E}})_{i,j} = 0 \quad \text{for all } j \text{ if } e_i \text{ is a self-loop},$$

$$(\mathscr{I}_{\mathbb{T}})_{i,j} = \begin{cases} 1 & \text{if } \ell_i \text{ is incident to } v_j \\ 0 & \text{if } \ell_i \text{ is not incident to } v_j. \end{cases}$$

Introduce the vector of vertex potentials $V_{\mathbb{V}}$, of edge currents $E_{\mathbb{E}}$, of leaf (external terminal) potentials V, and of leaf (external terminal) currents I

$$V_{\mathbb{V}} = \begin{bmatrix} V_{v_1} \\ V_{v_2} \\ \vdots \\ V_{v_{|\mathbb{V}|}} \end{bmatrix}, \quad I_{\mathbb{E}} = \begin{bmatrix} I_{e_1} \\ I_{e_2} \\ \vdots \\ I_{e_{|\mathbb{E}|}} \end{bmatrix}, \quad V = \begin{bmatrix} V_{t_1} \\ V_{t_2} \\ \vdots \\ V_{t_{|\mathbb{T}|}} \end{bmatrix}, \quad I = \begin{bmatrix} I_{t_1} \\ I_{t_2} \\ \vdots \\ I_{t_{|\mathbb{T}|}} \end{bmatrix}. \quad (1)$$

Introduce also the *edge resistance matrix* $R \in [0,\infty)^{|\mathbb{E}|\times|\mathbb{E}|}$, the diagonal matrix with elements $\rho(e_1), \rho(e_2), \ldots, \rho(e_{|\mathbb{E}|})$ on the diagonal.

The behavioral equations of the circuit can be written compactly as

$$\mathscr{I}_{\mathbb{E}} V_{\mathbb{V}} + R I_{\mathbb{E}} = 0 \qquad \mathscr{I}_{\mathbb{E}}^{\top} I_{\mathbb{E}} + \mathscr{I}_{\mathbb{T}}^{\top} I = 0 \qquad \mathscr{I}_T V_{\mathbb{V}} = V. \quad (2)$$

Equations (2) specify the terminal behavior of the resistive circuit. The terminal voltage/current behavior is given by

$$\mathscr{B} = \{(V,I) \in \mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|} \mid \exists\ V_{\mathbb{V}} \in \mathbb{R}^{|\mathbb{V}|} \text{ and } I_{\mathbb{E}} \in \mathbb{R}^{|\mathbb{E}|} \text{ s.t. } (2)\}.$$

Since these equations are linear, the latent variables $V_{\mathbb{V}}$ and $I_{\mathbb{E}}$ can be completely eliminated, resulting in a set of linear relations

$$L_V V + L_I I = 0$$

for the manifest variables. The purpose of this paper is to point out the exact special nature of these equations resulting from the linear resistive nature of the circuit.

IV. The Main Result

Theorem 1: In a suitable ordering of the terminals of a linear resistive circuit, the equations governing the terminal behavior take the following specific form. There exist positive integers $N_1, N_2, \ldots, N_k$ with $N_1 + N_2 + \cdots + N_k = |\mathbb{T}|$ so that the behavioral equations take the form

$$\begin{aligned} V_{t_1} = V_{t_2} = \cdots = V_{t_{N_1}} &=: \tilde{V}_1 \\ V_{t_{N_1+1}} = V_{t_{N_1+2}} = \cdots = V_{t_{N_1+N_2}} &=: \tilde{V}_2 \\ \vdots \qquad\qquad\qquad\qquad &\quad \vdots \\ V_{t_{|\mathbb{T}|-N_k+1}} = V_{t_{|\mathbb{T}|-N_k+2}} = \cdots = V_{|\mathbb{T}|} &=: \tilde{V}_k \end{aligned} \quad (3)$$

$$\begin{aligned} \tilde{I}_1 &:= I_{t_1} + I_{t_2} + \cdots + I_{t_{N_1}} \\ \tilde{I}_2 &:= I_{t_{N_1+1}} + I_{t_{N_1+2}} + \cdots + I_{t_{N_1+N_2}} \\ &\vdots \qquad\qquad\qquad\qquad \vdots \\ \tilde{I}_k &:= I_{t_{|\mathbb{T}|-N_k+1}} + I_{t_{|\mathbb{T}|-N_k+2}} + \cdots + I_{|\mathbb{T}|} \end{aligned} \quad (4)$$

combined with

$$\begin{bmatrix} \tilde{I}_1 \\ \tilde{I}_2 \\ \vdots \\ \tilde{I}_k \end{bmatrix} = G \begin{bmatrix} \tilde{V}_1 \\ \tilde{V}_2 \\ \vdots \\ \tilde{V}_k \end{bmatrix}, \quad (5)$$

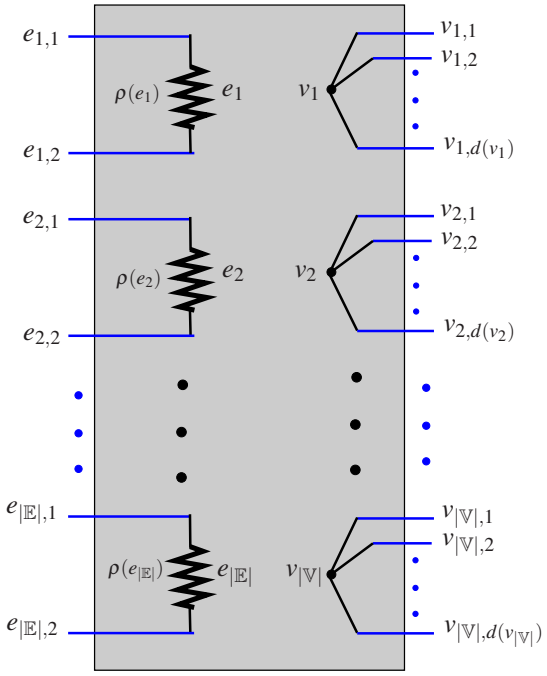
with $G \in \mathbb{R}^{k\times k}$ a square matrix satisfying

(i) $G_{i,i} \geq 0 \quad$ for $i = 1,2,\ldots,k$,
(ii) $G_{i,j} = G_{j,i} \leq 0 \quad$ for $i,j = 1,2,\ldots,k, i \neq j$
(iii) $\sum_{i=1}^{k} G_{i,j} = \sum_{j=1}^{k} G_{i,j} = 0 \quad$ for $i,j = 1,2,\ldots,k$.

Square matrices satisfying (i), (ii), and (iii) are called *symmetric hyperdominant with zero excess*.

Conversely, for a set of equations having the structure of equations (4, 5), with $G \in \mathbb{R}^{k\times k}$ symmetric hyperdominant with zero excess, there exists a linear resistive circuit with these terminal voltage/current behavioral equations.

V. Building a Circuit from its Components



In this section, we view a resistive circuit as an interconnection of (i) resitors and (ii) connectors. Each resistor has 2 terminals, while the connectors have a variable number of terminals, equal to the number of terminals it connects in the interconnected circuit.

The interconnection procedure lays at the basis of our proof of the main result, Theorem 1. We start with $|\mathbb{E}|$ resistors and $|\mathbb{V}|$ connectors, viewed as unconnected elements, as shown in the figure above. The resistors have resistances

$$\rho(e_1), \rho(e_2), \ldots, \rho(e_{|\mathbb{E}|}),$$

and the connectors have

$$d(v_1), d(v_2), \ldots, d(v_{|\mathbb{V}|})$$

terminals. Label the resistor terminals as

$$\mathbb{T}_{\mathscr{R}} = \{e_{1,1}, e_{1,2}, e_{2,1}, e_{2,2}, \cdots, e_{|\mathbb{E}|,1}, e_{|\mathbb{E}|,2}\}$$

and the connector terminals as

$$\begin{aligned}\mathbb{T}_{\mathscr{C}} \quad = \quad & \{v_{1,1}, v_{1,2}, \ldots, v_{1,d(v_1)}, v_{2,1}, v_{2,2}, \ldots, v_{2,d(v_2)}, \ldots, \\ & v_{|\mathbb{V}|,1}, v_{|\mathbb{V}|,2}, \ldots, v_{|\mathbb{V}|,d(v_{|\mathbb{V}|})}\}.\end{aligned}$$

Assume that $2|\mathbb{E}| + |\mathbb{T}| = d(v_1) + d(v_2) + \cdots + d(v_{|\mathbb{V}|})$. The *terminal interconnection assignment* $\mathscr{A}$ is a bijective map $\mathscr{A} : \mathbb{T}_{\mathscr{R}} \cup \{t_1, t_2, \ldots, t_{|\mathbb{T}|}\} \to \mathbb{T}_{\mathscr{C}}$. $\mathscr{A}$ associates with each connector terminal a resistor terminal or an external terminal, and specifies which resistor terminal is connected to which connector terminal, and which external terminal correspond to which connector terminal. In terms of the circuit architecture of Section II, $v_{k,\ell} = \mathscr{A}(e_{i,j})$ means that edge e_i is incident to vertex v_k, while $v_{k,\ell} = \mathscr{A}(i)$ means that leaf i is incident to vertex v_k.

The above construction leads to an alternative way of obtaining equations describing a resistive circuits. Introduce the resistor and connector terminal voltages and currents

$$\begin{aligned}&V_{e_1,1}, V_{e_1,2}, V_{e_2,1}, V_{e_2,2}, \ldots, V_{e_{|\mathbb{E}|},1}, V_{e_{|\mathbb{E}|},2}, \\ &I_{e_1,1}, I_{e_1,2}, I_{e_2,1}, I_{e_2,2}, \ldots, I_{e_{|\mathbb{E}|},1}, I_{e_{|\mathbb{E}|},2}, \\ &V_{v_1,1}, V_{v_1,2}, \ldots, V_{v_1,d(v_1)}, \ldots, V_{v_{|\mathbb{V}|},1}, V_{v_{|\mathbb{V}|},2}, \ldots, V_{v_{|\mathbb{V}|},d(v_{|\mathbb{V}|})}, \\ &I_{v_1,1}, I_{v_1,2}, \ldots, I_{v_1,d(v_1)}, I_{v_{|\mathbb{V}|},1}, I_{v_{|\mathbb{V}|},2}, \ldots, I_{v_{|\mathbb{V}|},d(v_{|\mathbb{V}|})}. \qquad (6)\end{aligned}$$

This leads to the following behavioral equations (recall that currents are counted positive when they run into the circuit). For the resistors, we have

$$\begin{bmatrix} I_{e_k,1} \\ I_{e_k,2} \end{bmatrix} = \begin{bmatrix} \rho(e_k)^{-1} & -\rho(e_k)^{-1} \\ -\rho(e_k)^{-1} & \rho(e_k)^{-1} \end{bmatrix} \begin{bmatrix} V_{e_k,1} \\ V_{e_k,2} \end{bmatrix} \qquad (7)$$

for $k = 1, 2, \cdots, |\mathbb{E}|$ such that $\rho(e_k) \neq 0$, and

$$V_{e_k,1} = V_{e_k,2} \qquad I_{e_k,1} + I_{e_k,2} = 0 \qquad (8)$$

for $k = 1, 2, \cdots, |\mathbb{E}|$ such that $\rho(e_k) = 0$. For the connectors, we have

$$V_{v_k,1} = V_{v_k,2} = \cdots = V_{v_k,d(v_k)} \qquad I_{v_k,1} + I_{v_k,2} + \cdots + I_{v_k,d(v_k)} = 0 \qquad (9)$$

for $k = 1, 2, \cdots, |\mathbb{V}|$. The terminal interconnections lead to

$$V_{e_k,\ell} = V_{\mathscr{A}(e_k,\ell)} \qquad I_{e_k,\ell} + I_{\mathscr{A}(e_k,\ell)} = 0 \qquad (10)$$

for $k = 1, 2, \cdots, |\mathbb{E}|, \ell = 1, 2, \ldots, |\mathbb{T}|$. Finally, the assignment of the external terminals leads to

$$V_{t_i} = V_{\mathscr{A}(t_i)} \qquad I_{t_i} = I_{\mathscr{A}(t_i)} \qquad (11)$$

for $i = 1, 2, \cdots, |\mathbb{T}|$.

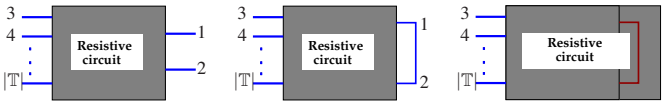
Equations (7, 8, 9, 10, 11) specify the terminal voltage/current behavior of a resistive circuit. As is common when modeling interconnected systems, these equations contain auxiliary 'latent' variables (the potentials and currents (6)) in addition to the 'manifest' variables (the terminal voltages and currents V, I) which the model aims at. Since these equations are linear, the latent variables variables can be completely eliminated. Theorem 1 points out the exact special nature of the equations for the manifest variables resulting from the linear resistive nature of the circuit.

VI. Proof of Theorem 1

The proof consists of three main steps. In the first step, we prove that if we connect two terminals of a resistive circuit satisfying the structure of the equations of Theorem 1, and subsequently eliminate the potentials and currents of the two connected terminals, then the voltage/current equations for the remaining terminals keep the structure of the equations of Theorem 1. The second step uses the first step and the circuit description of Section V in order to arrive at equations with the structure given in Theorem 1. In the third step, the converse part of the theorem is proven.

A. Step 1: Terminal connection

The procedure followed is illustrated in the figure below. We start with a circuit with N terminals, as shown on the



left hand side of the figure. Subsequently, we connect two terminals, say terminals 1 and 2, as shown in the middle part of the figure, and obtain a circuit with $N-2$ terminals, as shown on the right hand side. We will prove that if the voltage/current terminal behavior of the circuit with N terminals is given by behavioral equations according to the structure of Theorem 1, then, after elimination of the potentials and currents of the two connected terminals, the voltage/current terminal behavior of the circuit with $N-2$ terminals is given by behavioral equations that also have this structure.

We consider two cases.

Case 1: Assume first that the connected terminals belong to the same cluster of equation (4). Without loss of generality, take the interconnected terminals to be terminals 1 and 2 and $N_1 \geq 2$. The interconnection equations resulting from connecting these terminals are given by

$$V_1 = V_2 \qquad I_1 + I_2 = 0. \qquad (12)$$

These equations impose restrictions on the variables V_1, V_2, I_1, I_2. The question is to obtain the conditions on the remaining terminal variables imposed by equations (4, 5, 12). We now consider again 2 cases.

Case 1.1: $N_1 > 2$. Then the equations for the remaining variables are

$$\begin{aligned} V_3 = V_4 = \cdots = V_{N_1} &=: \tilde{V}_1 \\ V_{N_1+1} = V_{N_1+2} = \cdots = V_{N_1+N_2} &=: \tilde{V}_2 \\ \vdots \qquad\qquad & \vdots \\ V_{|\mathbb{T}|-N_k+1} = V_{|\mathbb{T}|-N_k+2} = \cdots = V_{|\mathbb{T}|} &=: \tilde{V}_k \end{aligned}$$

$$\begin{aligned}\tilde{I}_1 &:= I_3 + I_4 + \cdots + I_{N_1}\\ \tilde{I}_2 &:= I_{N_1+1} + I_{N_1+2} + \cdots + I_{N_1+N_2}\\ &\vdots \qquad\qquad \vdots\\ \tilde{I}_k &:= I_{|\mathbb{T}|-N_k+1} + I_{|\mathbb{T}|-N_k+2} + \cdots + I_{|\mathbb{T}|}\end{aligned}$$

combined with equation (5). Clearly these equations have the structure of the equations given in Theorem 1.

Case 1.2: $N_1 = 2$. Then we obtain the equations

$$\begin{aligned}V_1 = V_2 &=: \tilde{V}_1\\ V_{N_1+1} = V_{N_1+2} = \cdots = V_{N_1+N_2} &=: \tilde{V}_2\\ &\vdots \qquad\qquad \vdots\\ V_{|\mathbb{T}|-N_k+1} = V_{|\mathbb{T}|-N_k+2} = \cdots = V_{|\mathbb{T}|} &=: \tilde{V}_k\end{aligned}$$

$$\begin{aligned}0 &= I_1 + I_2\\ \tilde{I}_2 &:= I_{N_1+1} + I_{N_1+2} + \cdots + I_{N_1+N_2}\\ &\vdots \qquad\qquad \vdots\\ \tilde{I}_k &:= I_{|\mathbb{T}|-N_k+1} + I_{|\mathbb{T}|-N_k+2} + \cdots + I_{|\mathbb{T}|}\end{aligned}$$

combined with

$$\begin{bmatrix}0\\ \tilde{I}_2\\ \vdots\\ \tilde{I}_k\end{bmatrix} = G \begin{bmatrix}\tilde{V}_1\\ \tilde{V}_2\\ \vdots\\ \tilde{V}_k\end{bmatrix}$$

We need to eliminate V_1, V_2, I_1, I_2, and $\tilde{V}_1$ from these equations. We distinguish again two cases.

Case 1.2.1: $G_{1,1} = 0$. This implies $G_{i,1} = G_{1,i}$ for $i = 1, 2, \cdots, k$. Then elimination is immediate, leading to the behavioral equations

$$\begin{aligned}V_{N_1+1} = V_{N_1+2} = \cdots = V_{N_1+N_2} &=: \tilde{V}_2\\ V_{N_1+N_2+1} = V_{N_1+N_2+2} = \cdots = V_{N_1+N_2+N_3} &=: \tilde{V}_3\\ &\vdots \qquad\qquad \vdots\\ V_{|\mathbb{T}|-N_k+1} = V_{|\mathbb{T}|-N_k+2} = \cdots = V_{|\mathbb{T}|} &=: \tilde{V}_k\end{aligned}$$

$$\begin{aligned}\tilde{I}_2 &:= I_{N_1+1} + I_{N_1+2} + \cdots + I_{N_1+N_2}\\ \tilde{I}_3 &:= I_{N_1+N_2+1} + I_{N_1+N_2+2} + \cdots + I_{N_1+N_2+N_3}\\ &\vdots \qquad\qquad \vdots\\ \tilde{I}_k &:= I_{|\mathbb{T}|-N_k+1} + I_{|\mathbb{T}|-N_k+2} + \cdots + I_{|\mathbb{T}|}\end{aligned}$$

combined with

$$\begin{bmatrix}\tilde{I}_2\\ \tilde{I}_3\\ \vdots\\ \tilde{I}_k\end{bmatrix} = \hat{G} \begin{bmatrix}\tilde{V}_2\\ \tilde{V}_3\\ \vdots\\ \tilde{V}_k\end{bmatrix}$$

with the matrix $\hat{G} \in \mathbb{R}^{(k-1)\times(k-1)}$ derived from G by deleting the first row and the first column. It is easily verified that $\hat{G}$ is symmetric hyperdominant with zero excess. Hence these equations have the structure of the equations given in Theorem 1.

Case 1.2.2: $G_{1,1} \neq 0$. Then elimination leads to the behavioral equations

$$\begin{aligned}V_{N_1+1} = V_{N_1+2} = \cdots = V_{N_1+N_2} &=: \tilde{V}_2\\ V_{N_1+N_2+1} = V_{N_1+N_2+2} = \cdots = V_{N_1+N_2+N_3} &=: \tilde{V}_3\\ &\vdots \qquad\qquad \vdots\\ V_{|\mathbb{T}|-N_k+1} = V_{|\mathbb{T}|-N_k+2} = \cdots = V_{|\mathbb{T}|} &=: \tilde{V}_k\end{aligned}$$

$$\begin{aligned}\tilde{I}_2 &:= I_{N_1+1} + I_{N_1+2} + \cdots + I_{N_1+N_2}\\ \tilde{I}_3 &:= I_{N_1+N_2+1} + I_{N_1+N_2+2} + \cdots + I_{N_1+N_2+N_3}\\ &\vdots \qquad\qquad \vdots\\ \tilde{I}_k &:= I_{|\mathbb{T}|-N_k+1} + I_{|\mathbb{T}|-N_k+2} + \cdots + I_{|\mathbb{T}|}\end{aligned}$$

combined with

$$\begin{bmatrix}\tilde{I}_2\\ \tilde{I}_3\\ \vdots\\ \tilde{I}_k\end{bmatrix} = \hat{G} \begin{bmatrix}\tilde{V}_2\\ \tilde{V}_3\\ \vdots\\ \tilde{V}_k\end{bmatrix}.$$

The matrix $\hat{G}$ is the Schur complement of $G_{1,1}$ in G, given by

$$\hat{G} = \tilde{G} - \frac{aa^\top}{G_{1,1}}$$

with $G_{1,1}, a,$ and $\tilde{G}$ derived from G by

$$G = \begin{bmatrix}G_{1,1} & a^\top\\ a & \tilde{G}\end{bmatrix}.$$

It is readily verified that $\hat{G}$ is symmetric and hyperdominant with zero excess. These equations are hence of the form of the equations given in Theorem 1.

Case 2: Assume next that the connected terminals belong to different clusters of equation (4). Without loss of generality, take the interconnected terminals to be terminals 1 and $N_1 + 1$. The interconnection equations resulting from connecting these terminals are given by

$$V_1 = V_{N_1+1} \qquad I_1 + I_{N_1+1} = 0. \tag{13}$$

These equations impose restrictions on the variables $V_1, V_{N_1+1}, I_1, I_{N_1+1}$. The question now is to obtain the conditions on the remaining variables imposed by equations (4, 5, 13). The proof that the resulting equations are of the form of the equations given in Theorem 1 is similar to Case 1, and is left out for space limitations.

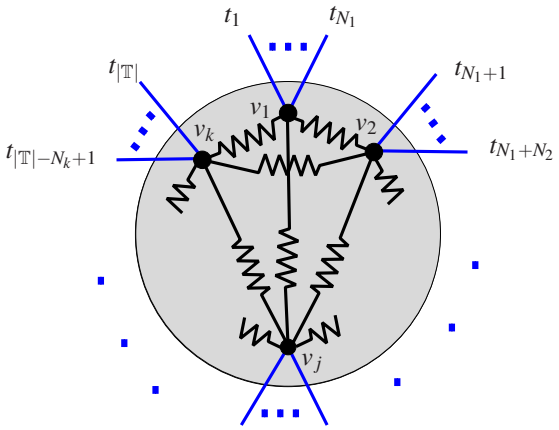
B. Step 2: Connecting terminals one at the time

Start with the circuit shown in the figure of Section V with the variables displayed in (6) viewed as the terminal variables. These variables are governed by equations (7, 8, 9). Clearly these equations have the structure of the equations of Theorem 1. Now connect the terminals one at the time. This corresponds to applying one the equations (10). Each time, eliminate the voltages and currents of the connected terminals. By Section VI-A, this leads each time to equations that have the structure of the equations of

Theorem 1. This process goes on until only the terminals $\mathscr{A}(t_1),\mathscr{A}(t_2),\ldots,\mathscr{A}(t_{|\mathbb{T}|})$ of the connectors remain as terminal variables. Finally substitute the external variables, using equations (11). This proves that the equations of the terminal behavior of a linear resistive circuit have the structure of the equations of Theorem 1.

C. Step 3: Proof of the converse

The converse is obtained by the circuit shown in the figure below. This circuit has k vertices, the same number of edges



as there are non-zero non-diagonal elements in the matrix G, and N leaves. The leaves $1,2,\cdots,N_1$ are incident to vertex v_1, the leaves $N_1+1,N_1+2,\cdots,N_1+N_2$ are incident to vertex v_2, ... , and the leaves $N-N_k+1,N-N_k+2,\cdots,N$ are incident to vertex v_k. The edge corresponding to the non-zero element $G_{i,j},i\neq j$, is incident to vertices v_i and v_j, and the associated resistance is $-\frac{1}{G_{i,j}}$.

VII. Decomposition

Using a property of matrices that are symmetric hyperdominant with zero excess leads to the following more structured version of Theorem 1.

Theorem 2: In a suitable ordering of the terminals of a linear resistive circuit, the equations governing the terminal behavior take the following specific form. There exist positive integers $N_1,N_2,\ldots,N_k$ with $N_1+N_2+\cdots+N_k=|\mathbb{T}|$ leading to the first set of behavioral equations as (4)

$$\begin{aligned} V_1=V_2=\cdots=V_{N_1}&=:\tilde{V}_1\\ V_{N_1+1}=V_{N_1+2}=\cdots=V_{N_1+N_2}&=:\tilde{V}_2\\ \vdots\qquad\qquad&\vdots\\ V_{|\mathbb{T}|-N_k+1}=V_{|\mathbb{T}|-N_k+2}=\cdots=V_{|\mathbb{T}|}&=:\tilde{V}_k \end{aligned}$$

$$\begin{aligned} \tilde{I}_1&:=I_1+I_2+\cdots+I_{N_1}\\ \tilde{I}_2&:=I_{N_1+1}+I_{N_1+2}+\cdots+I_{N_1+N_2}\\ &\vdots\qquad\qquad\vdots\\ \tilde{I}_k&:=I_{|\mathbb{T}|-N_k+1}+I_{|\mathbb{T}|-N_k+2}+\cdots+I_{|\mathbb{T}|} \end{aligned}$$

integers $k_1,k_2,\ldots,k_m$ with $k_1+k_2+\cdots+k_m=k$ leading to

$$\tilde{\tilde{V}}_1:=\begin{bmatrix}\tilde{V}_1\\ \tilde{V}_2\\ \vdots\\ \tilde{V}_{k_1}\end{bmatrix},\tilde{\tilde{I}}_1:=\begin{bmatrix}\tilde{I}_1\\ \tilde{I}_2\\ \vdots\\ \tilde{I}_{k_1}\end{bmatrix},\ldots,\tilde{\tilde{V}}_m:=\begin{bmatrix}\tilde{V}_{k-k_m+1}\\ \tilde{V}_{k-k_m+2}\\ \vdots\\ \tilde{V}_k\end{bmatrix},\tilde{\tilde{I}}_m:=\begin{bmatrix}\tilde{I}_{k-k_m+1}\\ \tilde{I}_{k-k_m+2}\\ \vdots\\ \tilde{I}_k\end{bmatrix} \tag{14}$$

The variables $\tilde{\tilde{V}}_i$ and $\tilde{\tilde{I}}_i$ are related by

$$\tilde{\tilde{I}}_i=G_i\,\tilde{\tilde{V}}_i,\quad \text{for } i=1,2,\cdots,m, \tag{15}$$

with $G_i\in\mathbb{R}^{k_i\times k_i}$ symmetric hyperdominant with zero excess, and $\mathtt{rank}(G_i)=k_i-1$ for $i=1,2,\cdots,m$.

Theorem 2 states that in a suitable ordering of the terminals of a linear resistive circuit, the behavioral equation (5) appearing in Theorem 1 can be further refined so that

$$G=\begin{bmatrix}G_1&0&\cdots&0\\ 0&G_2&\cdots&0\\ \vdots&\vdots&\vdots&\vdots\\ 0&0&\cdots&G_m\end{bmatrix} \tag{16}$$

with each of the G_i's matrices that are symmetric hyperdominant with zero excess and of rank deficiency 1.

Theorem 2 follows from Theorem 1 combined with the following proposition.

Proposition 3: Let $G\in\mathbb{R}^{k\times k}$ be symmetric hyperdominant with zero excess. Assume that $\mathtt{rank}(G)=k-m$. Then there exists a permutation matrix $P\in\mathbb{R}^{k\times k}$ such that

$$P^\top GP=\begin{bmatrix}G_1&0&0&\cdots&0\\ 0&G_2&0&\cdots&0\\ 0&0&G_3&\cdots&0\\ \vdots&\vdots&\vdots&\ddots&\vdots\\ 0&0&0&\cdots&G_m\end{bmatrix}$$

with $G_i\in\mathbb{R}^{k_i\times k_i},\mathtt{rank}(G_i)=k_i-1$, and $k_1,k_2,\cdots,k_m$ positive integers such that $k_1+k_2+\cdots k_m=k$.

VIII. Shorted and connected terminals

We now explain the presence of equations (4) and of the clustering (14) in terms of properties of the graph with leaves that define the circuit architecture as defined in Section II. We consider two equivalence relations on the external terminals.

For a graph with leaves $\mathscr{G}$, a *path from leaf* $\ell_i\in\mathbb{L}$ *to leaf* $\ell_j\in\mathbb{L}$ is defined as a sequence $(\ell_i,v_{k_1},e_{k'_1},v_{k_2},e_{k'_2},\ldots,v_{k_{n-1}},e_{k'_{n-1}},v_{k_n},\ell_j)$ where $v_{k_m}\in\mathbb{V}$ for $m=1,2,\ldots,n$, and $e_{k'_m}\in\mathbb{E}$ for $m=1,2,\ldots,n-1$, with ℓ_i incident to v_{k_1}, with v_{k_m} and $v_{k_{m+1}}$ incident to e_{k_m} for $m=1,2,\ldots,n-1$, and with ℓ_j incident to v_{k_n}. A path $(\ell_i,v_{k_1},e_{k'_1},v_{k_2},e_{k'_2},\ldots,v_{k_{n-1}},e_{k'_{n-1}},v_{k_n},\ell_j)$ from terminal i to terminal j of a resistive circuit is said to be a *zero resistance path* if either $n=1$ or $\rho(e_{k'_m})=0$ for $m=1,2,\ldots,n-1$.

Terminals i and j of a linear resistive circuit are said to be *connected* if there exists a path from the leaf corresponding to terminal i to the leaf corresponding to terminal j, and *shorted* if there exists a zero resistance path from the leaf corresponding to terminal i to the leaf corresponding to terminal j. Both connectedness and being shorted define an equivalence relation on the terminals of a linear resistive circuit. Since

shorted implies connected, the partition corresponding to the equivalence relation due to terminals being shorted is a refinement of the partition corresponding to the equivalence relation due to terminals being connected.

Equation (4) of Theorem 1 defines a partition of the terminals into the sets

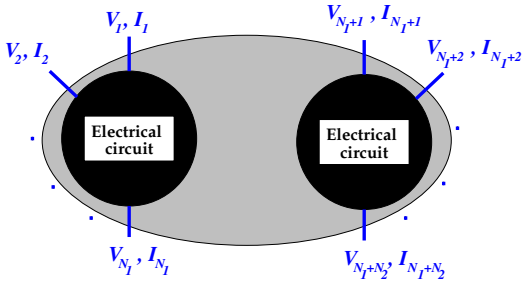
$$\{1,2,\ldots,N_1\},\{N_1+1,N_1+2,\ldots,N_1+N_2\},\ldots,$$
$$\ldots,\{|\mathbb{T}|-N_k+1,|\mathbb{T}|-N_k+2,\cdots,|\mathbb{T}|\}.$$

It is easy to prove that this partition corresponds exactly to the partition induced by the equivalence relation of being shorted. Equation (14) of Theorem 2 defines also a partition of the terminals into the sets

$$\{1,2,\ldots,N_1+N_2+\cdots+N_{k_1}\},$$
$$\{N_1+N_2+\cdots+N_{k-k_m}+1,N_1+\cdots+N_{k-k_m}+2,\ldots,|\mathbb{T}|\}.$$

It is easy to prove that this second partition, obviously more coarse than the first one, corresponds exactly to the partition induced by the equivalence relation of being connected.

Let $\mathscr{B}\subseteq\mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|},\mathscr{B}_1\subseteq\mathbb{R}^{N_1}\times\mathbb{R}^{N_1}$, and $\mathscr{B}_2\subseteq\mathbb{R}^{N_2}\times\mathbb{R}^{N_2}$ be the voltage/current terminal behavior of memoryless circuits with respectively $|\mathbb{T}|=N_1+N_2,N_1$, and N_2 terminals. If, after a suitable reordering of the terminals, there holds $\mathscr{B}=\mathscr{B}_1\times\mathscr{B}_2$, then we call $(\mathscr{B}_1,\mathscr{B}_2)$ a *decomposition* of $\mathscr{B}$. Note that a decomposition corresponds to viewing a circuit as two or more circuits that act completely independently, as illustrated in the figure below. A linear resistive circuit is



said to be *indecomposable* if it cannot be decomposed into two or more linear resistive circuits.

Theorem 4: Consider a linear resistive circuit, governed, following Theorem 1, by the behavioral equations (4, 5). Assume that no two terminals are shorted. Let $\mathtt{rank}(G)=|\mathbb{T}|-m$. Then the circuit can be decomposed in m indecomposable linear resistive circuits following the decomposition of Theorem 2. Two terminals belong to the same component if and only if they are connected. A circuit is indecomposable if and only if $\mathtt{rank}(G)=|\mathbb{T}|-1$, equivalently, if and only if every two terminals are connected.

Theorem 5: Consider a linear resistive circuit. The equations governing the terminal behavior take the following form $I=G\,V$, with $G\in\mathbb{R}^{k\times k}$ a square matrix which is symmetric hyperdominant with zero excess if and only if no two distinct terminals are shorted.

These theorems are readily proven using the procedure explained in Section VI-B.

A linear resistive circuit is said to be *simple* if no two terminals are shorted and every two terminals are connected.

Theorem 6: A linear resistive circuit is simple if and only if it is described by behavioral equations of the form $V=GI$, with $G\in\mathbb{R}^{N\times N}$ symmetric hyperdominant with zero excess and $\mathtt{rank}(G)=N-1$.

IX. Conclusions

The terminal voltage/current behavior of a purely linear resistive circuit was derived, and the special nature of the equations relating the terminal voltages and terminal currents was characterized. The matrix G in the relation was found to be symmetric hyperdominant with zero excess. In contrast to the port description, the behavioral description of the terminals is more relevant when interconnections are made. The decomposition of a resistive circuit into a set of indecomposable components was discussed.

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