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Practical Implementation of a General Computer Aided Design Technique for Switched Capacitor Circuits

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Abstract—**In this paper a general and efficient CAD method for simulation of switched capacitor filters and A/D and D/A converters, is demonstrated. It is based on the direct implementation of controlled switch branches into the widely used modified nodal analysis technique and is therefore in contrast to other methods, directly compatible with existing CAD techniques. It allows for dc, time domain, and frequency response calculations for arbitrary clock cycles and all types of inputs (piecewise constant, sample and hold, and continuous). The circuit can also contain resistors and allows for nonlinear time domain analysis too.**

As implemented in the DIANA program it allows for full top-down design from principle to transistor level, including clock drivers, control logic, etc. Input is directly from the circuit diagram. The method is illustrated by practical design examples.

I. Introduction

In the last few years, switched capacitor circuits have been successfully used for the design of single chip metal–oxide–semiconductor–large-scale integration (MOS-LSI) filters and A/D and D/A convertors [1]-[4]. This technique has caused a breakthrough of analog LSI signal processing. Research for adequate CAD tools for such circuits is motivated by the present lack of adequate design procedures and a large number of parasitic effects such as clock-feedthrough, offset, drift, stray capacitance, nonlinearities, aliasing, and noise problems.

These systems are indeed hard to simulate by existing CAD programs due to the very large ratio between sample and signal frequency which leads to excessive central processing unit (CPU) time for time domain analysis.

Another problem is that these circuits are basically time-variant circuits and although in the past [5], [6] and recently [7]-[9] analysis techniques for switched networks have been described, none of these methods are directly compatible with today's CAD programs and/or are restricted to a given class of clock sequences (e.g., two-phase clocks). They require the setup of a number of different matrices for the different clock phases [7], [9], are difficult to generate from the network description, and do not allow for switched capacitor networks containing resistive dividers. Furthermore, they do not allow for the study of clock-feedthrough, nonlinear, and parasitic effects.

In this paper a general method overcoming all the above restrictions is presented. Crucial to the method is the introduction in Section II of controlled switch branches into a single modified nodal admittance (MNA) matrix. These branches ranging from ideal switched to full MOS models can be introduced in any circuit simulator based on MNA (e.g., SPICE2 [15], ASTAP [16], DIANA [12], [17]). It will be shown that there is no restriction on the clocking sequence. Classical detailed resistive response using numerical integration is possible as well as a 1 calculation/clock phase analysis using charge conservation. It is shown that the latter case can be introduced with only minor modification in existing CAD programs. Nonlinear as well as resistive voltage division effects, can also be included (Section III).

Implemented in mixed-mode simulator DIANA [12], mixed analog digital circuits can be analyzed as demonstrated in Section III, case B. In Section IV a general method for frequency analysis using arbitrary inputs is demonstrated based on a simple example, and applications to practical circuits are given. In contrast to, e.g., the DINAP-program [19], the input description to DIANA follows immediately from topology, and no modeling or transposition of the circuit into a digital filter structure is needed. Also continuous inputs can be handled in the frequency domain, while programs as DINAP are essentially limited to piecewise constant inputs.

The implementation of the method in DIANA leads to a fully operational top-down design tool for mixed analog–digital MOS-LSI circuits.

II. Implementation of Switched Capacitor Networks in Existing CAD Programs

Crucial to the simulation method to be presented is the introduction of a hierarchical set of switch branches into the MNA-formalism, which is used in most existing CAD programs [13].

This method allows for a simple topological description of the network and is extremely simple to implement. We will start by looking at switched capacitor networks $\mathfrak{N}_{SC}$ consisting (for the time being) of ideal switches (S), capacitors (C), and dependent (A) and independent (E) voltage sources. This is no direct restriction since all practical switch capacitor

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networks are based on a sequence of equilibrium states. The design of detailed circuitry to satisfy the speed requirements can be done in a "top-down" fashion by simulating critical parts at a more detailed transistor level (see Section III, case B). Consider now a node i of a $\mathfrak{N}_{SC}$ network to which all the above elements are connected (Fig. 1). An ideal switch S is controlled by a Boolean clock variable $\phi_S \in \{0,1\}$. $\phi_S = 0$ and $\phi_S = 1$ correspond to an open, respectively closed, switch. Let $v_i^{(k)}$ be the voltage at node i at the end of the time interval $\Delta^{(k)}$ and let $q_j^{(k)}$ be the charge transferred in branch j during the time interval $\Delta^{(k)}$. The clock states (Fig. 1) define a time sequence $\tau = \{t_0, t_1 \cdots t_{k-1}, t_k \cdots\}$ and time slots $\Delta^{(1)} \cdots \Delta^{(k)}$, etc. We further assume that the independent voltage sources $E(t)$ only change value at the switching instants $t_k \in \tau$ and call them piecewise constant [7], i.e., $E(t \in [t_{k-1}, t_k]) = E^{(k)}$. This restriction will be removed later [see (5)]. Under the above conditions, and similar to the MNA method [13], currently used in most CAD programs, an independent set of equations for a transition from $\Delta^{(k-1)}$ to $\Delta^{(k)}$ consists of:

1) charge conservation in n independent nodes, e.g., in node i (Fig. 1):

$$Cv_i^{(k)} - Cv_j^{(k)} + q_A^{(k)} + q_E^{(k)} + \phi_S^{(k)} q_s^{(k)} = Cv_i^{(k-1)} - Cv_j^{(k-1)} \tag{1}$$

with

$$q_j^{(k)} = \int_{t_{k-1}}^{t_k} i_j(t)\, dt. \tag{2}$$

Equation (1) can also be obtained by integrating KCL at node i over the slot $\Delta^{(k)}$. This equation gives rise to row i in the MNA representation of Fig. 1(a) in Fig. 1(b);

2) branch relations for all E, A, and S. The branch relations for E and A are trivial from Fig. 1(b). Important is the implementation of switch branch S as follows:

$$\phi_S^{(k)} v_i^{(k)} - \phi_S^{(k)} v_k^{(k)} + \bar{\phi}_S^{(k)} q_S^{(k)} = 0, \tag{3}$$

$\bar{\phi}_S$ denotes the Boolean complement of ϕ_S.

From (1) and (3) it is clear how S is implemented into the matrix $\mathfrak{M}^{(k)}$. As shown by the dotted lines in Fig. 1(b) every element of $\mathfrak{N}_{SC}$ has a simple entry (stamp) into the matrix $\mathfrak{M}^{(k)}$ which is nothing but the widely used MNA [13] matrix now also including controlled switches and operating on a vector $X^{(k)}$ of voltages and charges.

Fig. 2 shows a number of voltage controlled switch branches, their implementation in the $\mathfrak{M}$ matrix, and their description in the DIANA program. The upper four branches are for $\mathfrak{N}_{SC}$ networks. The pass switch is a first-order MOS triode switch model for studying clock feedthrough and switching transient effects in classical transient analysis (see Section III). In contrast to previously published methods [7], [9] these switch models give a *direct* link between circuit design and single MNA matrix. Clearly no restriction is imposed on clock sequences which can be derived from, e.g., digital circuit parts (see Section III, case B). In closed form the equation in Fig. 1(b) can be written as

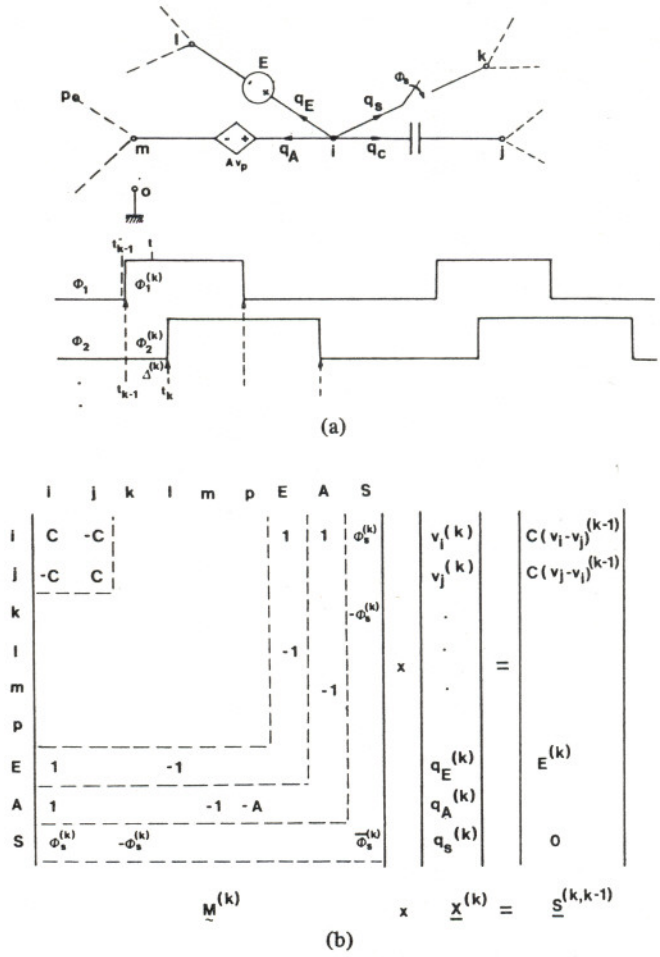


Fig. 1. (a) Resistorless switched capacitor network and clock definition. ϕ_i is a Boolean variable. t_{k-1}^- is the time immediately preceding the clock transition for time slot $\Delta^{(k)}$. (b) Matrix obtained from charge conservation and switch branches is an MNA matrix.

$$\mathfrak{M}^{(k)} X^{(k)} = S^{(k,k-1)}. \tag{4}$$

Equation (4) relates the soluting during $\Delta^{(k)}$ to the one during $\Delta^{(k-1)}$. $X^{(k)}$ can be solved by techniques discussed in [13].

If the signal sources $v_{\text{in}}{}^{(k)}$ are continuous instead of piecewise constant, i.e., $v_{\text{in}}(t)$, then it can easily be shown that (4) can be written as

$$\mathfrak{M}^{(k)} X^{(k)}(t) = S^{(k)}(t, t_{k-1}^-) \quad (t \in \Delta^{(k)}), \tag{5}$$

t_{k-1}^- is defined as in Fig. 1(a). Equations (4) and (5) will be of use in the Appendix.

Returning to Fig. 1(b) for piecewise constant inputs notice that the capacitor stamp is equivalent to the widely used backward Euler integration companion model for a capacitor for a *unit* time step [14]. This then leads to the following general simulation procedure for any switched capacitor network with arbitrary clock sequence and easy to implement in MNA based simulators:

1) introduce switch stamp as in Fig. 2;

2) use backward Euler integration with unit time step;

3) bypass all time step control. Time points coincide with clock sequence $t_0, t_1 \cdots t_k \cdots$;

4) start from inital values $v_C^{(0)}) = v_i^{(0)} - v_j^{(0)}$ for all capacitors. Default is zero;

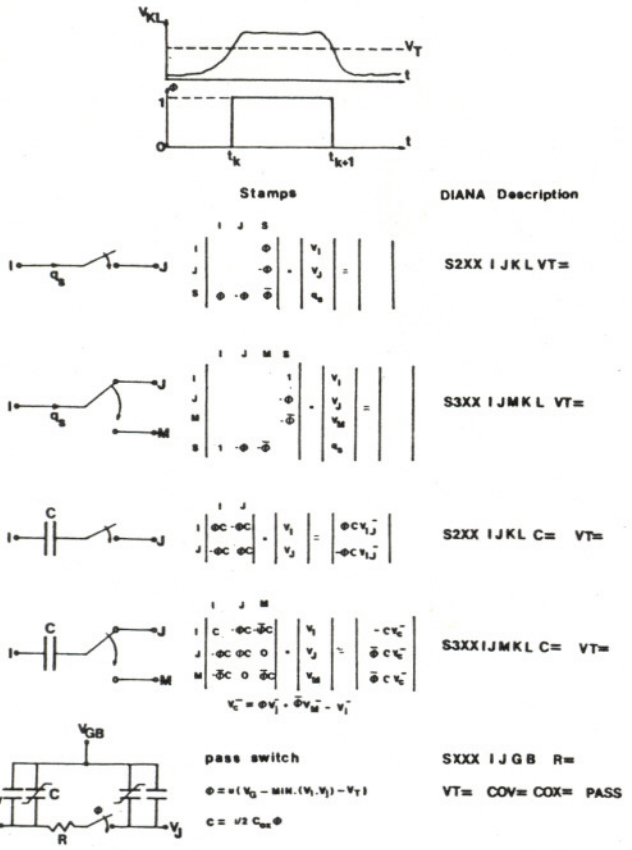


Fig. 2. Time controlled switch models used in DIANA. The pass switch is a first-order MOS triode model including channel charge effects.

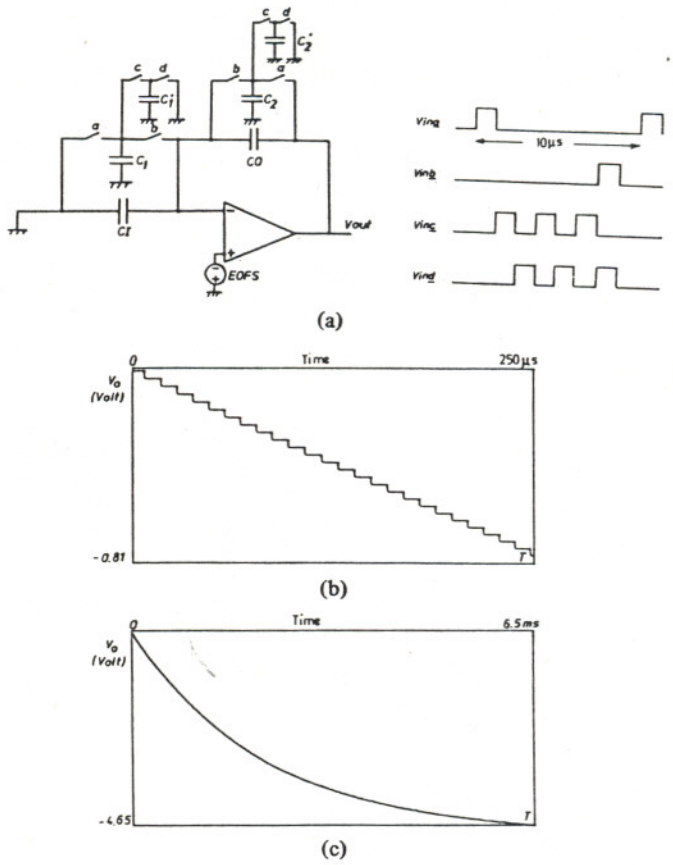


Fig. 3. Example of the simulation of offset caused drift. (a) Filter using charge redistribution in a subclock cycle. $C_I = 6$ pF, $C_2 = 6$ pF, $C_1' = 6.66$ pF, $C_2' = 16.6$ pF, $C_1 = C_0 = 20$ pF, $EOFS = 50$ mV. (b) Classical transient analysis result using pass switches for 25 clock cycles—1000 time points computed. (c) Result of new simulation method over 650 clock periods requiring the same computer time as (b) (30 s IBM 370/158).

5) generate (4) from topology description and solve for $X^{(k)}$;

6) interpret all $i^{(k)} \in X^{(k)}$ as $q^{(k)}$.

This method has been implemented in the DIANA program as an OPTION. A careful look at Fig. 1(b) also reveals that the method is fully compatible with the normal transient mode of simulation if backward Euler integration with $\Delta \neq 1$ is used and all q are taken as currents i.

Therefore in DIANA all modes of simulation from pure detailed transistor transient up to the above π_{SC} simulation are possible. Since DIANA also allows for mixed analog, timing, and logic simulation a full mixed analog-digital MOS-LSI circuit can be simulated as demonstrated in the following examples.

III. Linear and Nonlinear Time Response Calculations—Case Studies

Case A: Study of Offset Drift in a Switched C Network

Fig. 3(a) shows a possible method to avoid large capacitor ratios if a large pole-zero to sampling frequency is required.

Within the basic clock cycle ($V_{\text{in }a}$, $V_{\text{in }b}$) a charge redistribution using clocks ($V_{\text{in }c}$, $V_{\text{in }d}$) takes place on (C_1, C_1') and (C_2, C_2') comparable in magnitude to C_I and C_0. We want to study the influence of op amp offset, $EOFS = 50$ mV.

Fig. 3(b) shows the DIANA output plot of a *classical transient* analysis over 25 clock periods using PASS switch models. A 40 points/basic clock cycle has been used (1000 time steps).

Fig. 3(c) shows the result of the new MNA method over 650 clock periods, calculating 1 solution/time slot. The simulation reveals −4.65 V drift due to 50 mV offset of the op amp. This result was discovered by CAD and is caused by inadequate feedback of output offset errors by redistribution on (C_2, C_2'). Notice that the new method is ca. 26 times faster than classical transient analysis as both run times are the same (20 s CPU on IBM 370-158). If a nonlinear MOS model had been used, the difference would be about 100 ··· 150. Notice also that no problem occurs due to the complex clock sequence. The following example shows an application of fully mixed analog-digital simulation using pass switches.

Case B: Detailed Analysis of a Digitally Controlled Filter

Fig. 4(a) shows a pole-zero filter with a capacitor bank $C_1 \cdots C_4$ which can be digitally controlled by the user by an up-down command to accentuate or decrease frequencies in excess of 2.5 kHz (audio treble control filter). Fig. 4(b) shows the result of a hybrid transient analysis of the mixed analog-digital circuit using 1800 time steps of 1 μs, using pass-switch models and 1 pole op amp models (unity gain bandwidth: 1 MHz).

The input signal is a 10 kHz sine wave with an amplitude of 0.1 V.

Notice the clock-feedthrough effects on sample and hold, and the charge dumping spikes in op amp input. Spike A results

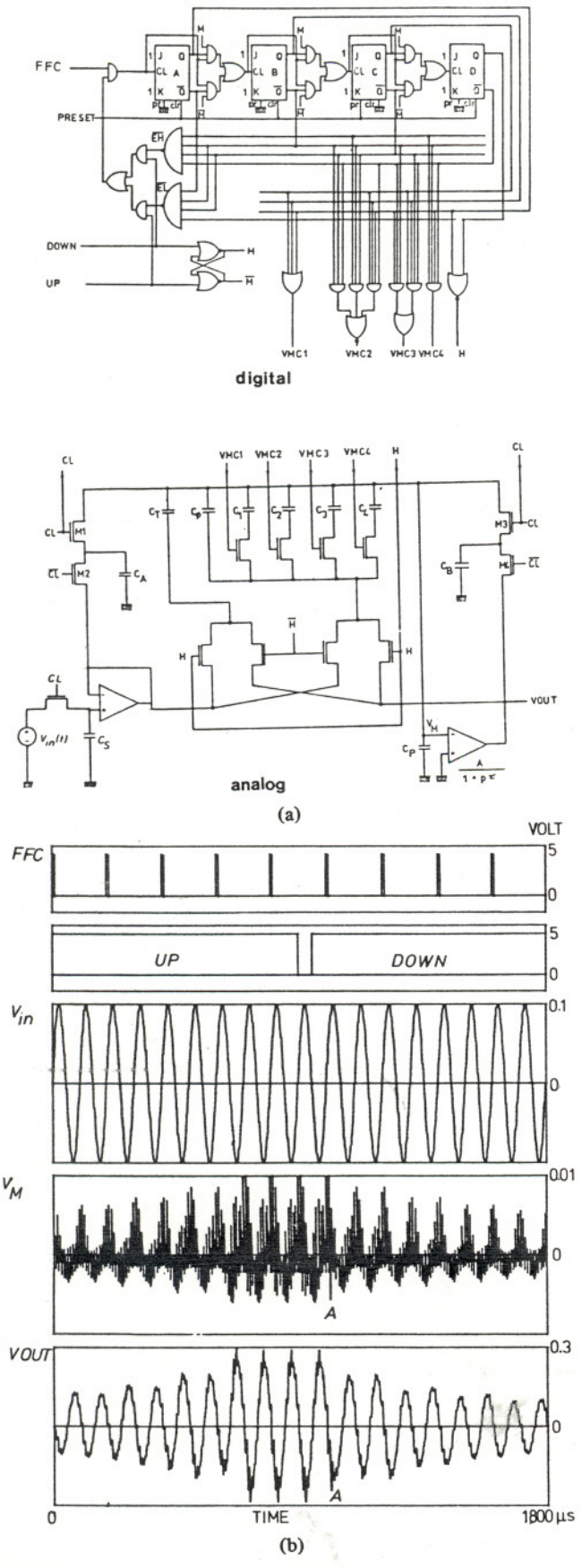


Fig. 4. Example of mixed-mode time domain simulation of a digitally controlled audio filter using pass switch models. (a) Circuit containing logic and analog parts. (b) Simulation of full circuit for a 10 kHz sinusoidal input V_{in}, digital inputs FFC, UP, and DOWN. Shown are the responses V_M (input op amp) and output V_{out} of the filter. $C_A = C_B = 4$ pF, $C_T = 30$ pF; $C_0 = 10$ pF, $C_{1 \ldots 4} = 5$ pF.

from a decoding hazard in the digital circuit whereby capacitances are switched in and out the feedback path in the analog circuit. This example takes 80 s CPU on an IBM 370-158 and can even be run on a minicomputer (PDP-11/40). This example clearly demonstrates how digital–analog interactions can be studied using the detailed analysis-mode which is still efficient due to the use of the pass-switch model.

Case C: Simulation of Nonlinear π_{SC} Networks

The above discussed method is not restricted to linear networks. Also nonlinear capacitors described by $q(v_c)$ can be simulated. Indeed (1) can be written as

$$q(v_c^{(k)}) + q_A^{(k)} + q_E^{(k)} + \phi_S q_S^{(k)} = q(v_c^{(k-1)}). \tag{6}$$

This is a nonlinear equation in $v_c^{(k)}$ which can be solved by the Newton–Raphson technique as used in all CAD programs. This leads to essentially the same method as for nonlinear backward-Euler with unit time step for capacitors. Also nonlinear gain of op amps can be introduced. A program which, e.g., handles backward-Euler nonlinear C's allows for direct simulation of nonlinear π_{SC} using the procedure in Section II.

Fig. 5 shows an example of an integrator with a nonlinear n-MOS junction capacitor as sample capacitor. The switches $S21$ and $S211$ are controlled by clock CL and operate in opposite phase. From the output plot we see that a 0.5 V amplitude sinusoidal input causes a drift and distortion in the output of the integrator. During the negative excursions (forward biased capacitor) more charge is exchanged than during the positive excursions. This simple example shows how offset, drift, and distortion effects due to nonlinearities can be studied.

The above examples clearly show how time domain simulation of switched capacitor networks is possible at all levels of detail. However in most cases a designer is interested in frequency response calculations to be discussed in the next paragraph.

IV. Simulation of the Frequency Response

In principle the frequency response of a pure sampled data circuit can be obtained from a fast Fourier transform (FFT) of the truncated unit sample response provided the latter is unique. However, since a switched capacitor circuit is a time variant circuit, a unique unit sample response does not always exist. Moreover the designer should be aware that switched capacitor circuits can have many different transfer functions depending on how and when one looks at the input and output signals of the filter.

In this paragraph we will use a simple example, shown in Fig. 6(a), to demonstrate how the frequency response can always be obtained from the FFT performed on the responses to a unit sample in each time slot $\Delta^{(k)}$ of the clock sequence. These can be obtained from a time domain simulation as discussed in Sections II and III.

We will consider first piecewise constant inputs and then the most general case of continuous inputs and direct capacitive I/O coupling.

A. Piecewise Constant Inputs

Consider the simple circuit in Fig. 6(a) which also shows the clocking sequence with time slots Δ_1 and Δ_2. As discussed in

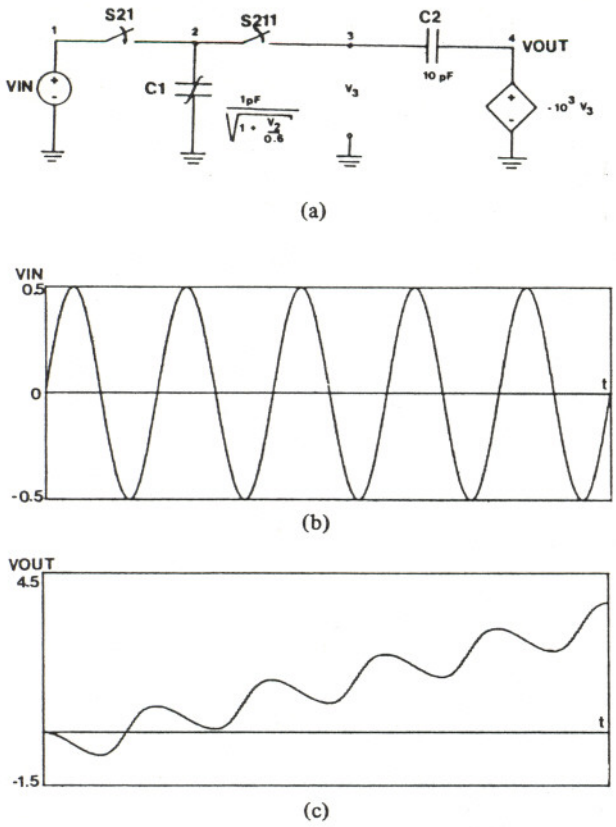


Fig. 5. Example of nonlinear switched capacitor network simulation. (a) An integrator with nonlinear sampling capacitor. (b) Sinusoidal input. (c) Simulated output waveform showing distortion and drift.

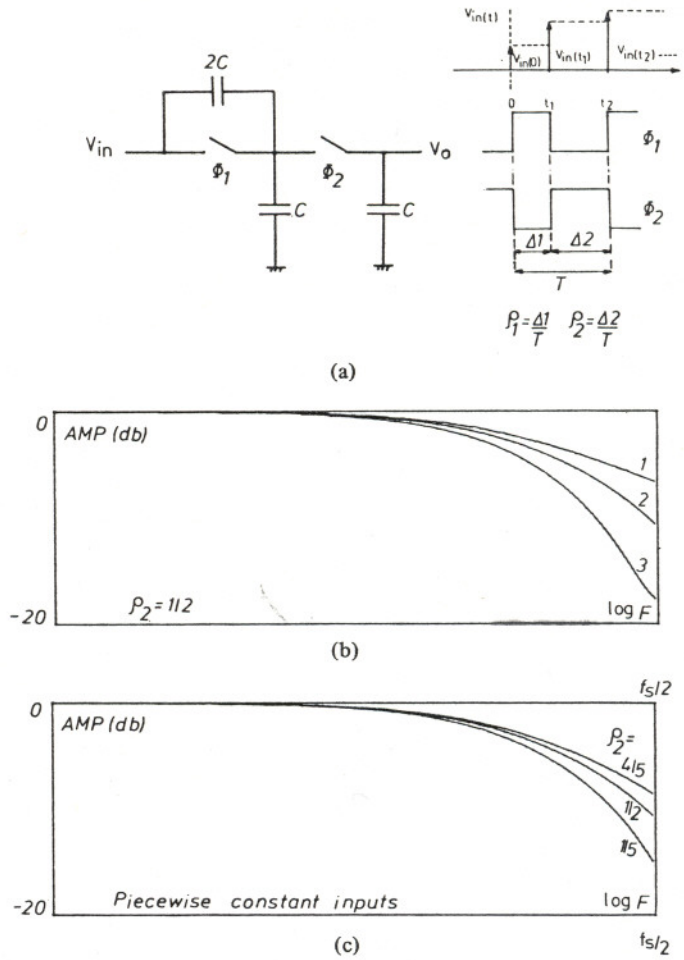


Fig. 6. Illustrative example showing different simulation modes. (a) Example circuit, its clocking sequence and piecewise constant input. (b) Simulated frequency response for duty cycle $\rho_2 = 0.5$ and output sampled at t_1 and held over T. Curve 1: for continuous input, Curve 2: for piecewise constant input, and Curve 3: for input sampled and held over period T. (c) For piecewise constant input and different ρ_2.

Section I a piecewise constant input for $v_{in}(t)$ is defined as $v_{in}(t)$ sampled at the beginning of each time slot and then held until the next time slot.

This defines samples $v_{in}(t_1 - T)$, $v_{in}(0)$, $v_{in}(t_1)$, $v_{in}(t_2) \cdots$ as shown in Fig. 6(a). It is common practice to consider the output as sampled only during one particular time slot [7] within the clock period T. For example in Fig. 6(a) it is natural to consider the output v_0 as sampled at $t_1 + nT$ (beginning of time slot Δ_2). Call this value $v_0(t_2)$.

For a piecewise constant input it is designers practice to write the difference equations of the circuit by inspection using charge conservation. This leads for Fig. 6(a) to

1) transition at 0:

$$v_0(0) = v_0(t_1 - T); \tag{7}$$

2) transition at t_1:

$$C(v_0(t_1) - v_0(0)) + C(v_0(t_1) - v_{in}(0)) + 2C(v_0(t_1) - v_{in}(t_1)) = 0. \tag{8}$$

From (7) and (8)

$$v_0(t_1) - \tfrac{1}{4} v_0(t_1 - T) = \tfrac{1}{2} v_{in}(t_1) + \tfrac{1}{4} v_{in}(0). \tag{9}$$

Let ω now be the pulsation of a sinusoidal input phasor $V_{in}(j\omega)$ of which the piecewise constant version is applied to the circuit and let $v_0^{(2)}(j\omega)$ be the phasor corresponding to this same pulsation in the output $v_0^{(2)}(t) = v_0(t_2)$ sampled during time slot Δ_2.[1] Then we can define the transfer function for the output sampled during Δ_2 as follows:

$$H_2(j\omega) = V_0^{(2)}(j\omega)/V_{in}(j\omega). \tag{10}$$

Using this practical definition and Fourier transform techniques one obtains

$$H_2(j\omega) = \frac{1/2}{1 - 1/4\, e^{-j\omega T}} + \frac{1/4\, e^{-j\omega \rho_1 T}}{1 - 1/4\, e^{-j\omega T}} \tag{11}$$

with $\rho_1 = \Delta_1/T$ as defined in Fig. 6(a).

We will now show how this transfer function can be obtained by the calculation of unit sample responses using the simulation method discussed in Sections II and III.

Indeed when driving the circuit with a unit sample input, respectively, on time slot Δ_1 and Δ_2 the time domain simulation gives the time series shown in Table I which can easily be verified by inspection of Fig. 6(a).

Table I clearly shows that two distinct unit sample responses

[1] Only the baseband spectrum is considered here.

TABLE I
UNIT SAMPLE RESPONSES FOR FIG. 6(a). δ_1 AND δ_2 ARE UNIT SAMPLES, RESPECTIVELY, DURING Δ_1 AND Δ_2. $h_1(t)$ AND $h_2(t)$ ARE THE SAMPLE RESPONSES. UNDERLINED ARE THE OUTPUTS SAMPLED AT TIME t_1 (TIME SLOT Δ_2).

	Δ_1	Δ_2	Δ_1	Δ_2	Δ_1	Δ_2	
	0	t_1	t_2	t_1+T	t_2+T	t_1+2T	t_2+2T	
δ_1	1	0	0	0	0	0	0	
$h_1(t)$	0	$\underline{1/4}$	1/4	$\underline{1/16}$	1/16	$\underline{1/64}$	$1/64\cdots$
δ_2	0	1	0	0	0	0	0	
$h_2(t)$	0	$\underline{1/2}$	1/2	$\underline{1/8}$	1/8	$\underline{1/32}$	$1/32\cdots$

TABLE II
UNIT SAMPLE RESPONSES AT Δ_2 RESULTING FROM UNIT SAMPLE AT Δ_1 AND Δ_2, RESPECTIVELY, AND THEIR FOURIER TRANSFORMS

$h_{2,1}(t)$	1/4	1/16	$1/64\cdots$	$H_{2,1}(e^{j\omega T}) = \frac{1}{4}\frac{1}{1-\frac{1}{4}e^{-j\omega T}}$	(12)
$h_{2,2}(t)$	1/2	1/8	$1/32\cdots$	$H_{2,2}(e^{j\omega T}) = \frac{1}{2}\frac{1}{1-\frac{1}{4}e^{-j\omega T}}$	(13)

sampled at $t_1 + n\bar{T}$ exist. We call them $h_{2,1}(t)$ and $h_{2,2}(t)$. They are represented in Table II together with their Fourier transforms $H_{2,1}(e^{j\omega T})$ and $H_{2,2}(e^{j\omega T})$ as obtained from the z transforms by using $z^{-1} = e^{-j\omega T}$.

Inspection of (11) and (12), (13) shows that

$$H_2(j\omega) = H_{2,2}(e^{j\omega T}) + e^{-j\omega t_1} H_{2,1}(e^{j\omega T}). \tag{14}$$

This is a natural result, since $h_{2,1}(t)$ results from an input signal sampled at the beginning of the previous time slot, i.e, a time t_1 earlier. This causes the phase factor $e^{-j\omega t_1}$ in (14).

Notice now that $H_{2,1}(e^{j\omega T})$, $H_{2,2}(e^{j\omega t})$ as well as $H_2(j\omega)$ can easily be obtained by applying an FFT algorithm to $h_{2,1}(t)$ and $h_{2,2}(t)$ resulting from a time domain simulation of the unit responses using the method of Sections II and III. If the output is sampled and held during period T (as is the case here) one has to multiply the FFT result (14) by

$$f = e^{-j\omega T/2}\frac{\sin(\omega T/2)}{\omega T/2}. \tag{15}$$

The result of a DIANA simulation of Fig. 6(a) for piecewise constant input, $\rho_2 = 0.5$, and the output sampled at t_1 and held over T are shown in Fig. 6(b), curve 2, whereas Fig. 6(c) shows a simulation for three different values of the duty cycle ρ_2. Clearly the duty cycle has a big influence on this circuit due to the phase effects it causes in the transfer function. The technique demonstrated here for a simple example can be generalized for all switched capacitor networks driven by piecewise continuous inputs as follows.

Consider the switched capacitor networks $\mathfrak{N}_s$ [see Fig. 7(a)] with clock signals $\phi_1 \cdots \phi_m$ defining l time slots Δ_i in each period T. The unit sample input on time slot i causes a time series on the output of $\mathfrak{N}_s$ [see Fig. 7(b)].

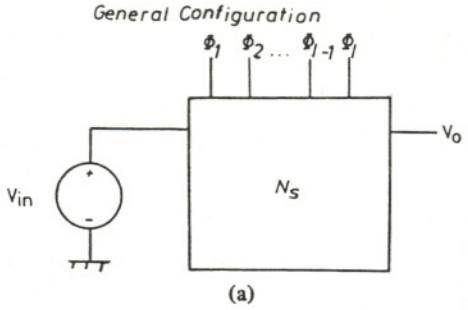
Observing the output only on time slot k of each period, a time series is generated [see Fig. 7(b)] of which the Fourier transform is $H_{k,i}(e^{j\omega T})$. This is the transfer function, similar to (10), from a sinusoidal input sampled in time slot i to the output, sampled in time slot k, and of which the phasor at the same frequency ω of the input is considered. This can be done in the same way for all time-slots i ($i = 1, l$) which leads to $H_{k,1}, H_{k,2} \cdots H_{k,l}$.

For the baseband frequencies ω then the total transfer function for time slot k, defined as $H_k(j\omega)$, can be obtained by superposition of the $H_{k,i}$ for $i = 1 \cdots l$ each multiplied with the phasefactor $e^{-j\omega(t_{k-1} - t_{i-1})}$ since they result from the sinusoidal input considered a time $t_{k-1} - t_{i-1}$ earlier or

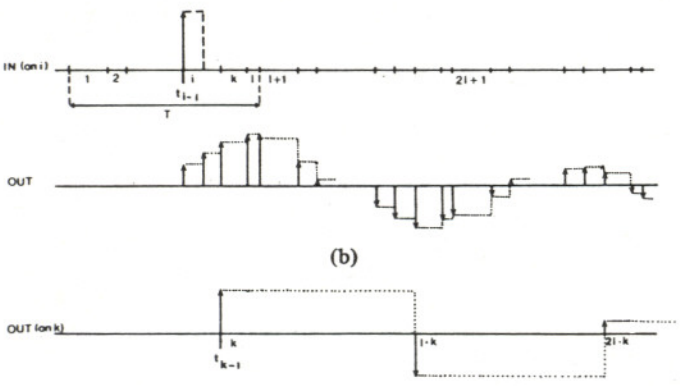
$$H_k(j\omega) = \sum_{k=1}^{l} H_{k,i}(e^{j\omega T}) \cdot e^{-j\omega(t_{k-1} - t_{i-1})}. \tag{16}$$

If sampled and held over period T, (16) still has to be multiplied by (15). Notice: 1) (16) is strictly only valid for the baseband (i.e., $0 < \omega < 2\pi/T$). A rigorous proof of (16), including full spectrum analysis, is beyond the scope of this paper and is the subject of a separate publication [11]; 2) (16) indicates that often different transfer functions are obtained dependent on the output sampling time slot.

The above described algorithm is built into the postprocessor of the DIANA program. It consists of the calculation of the



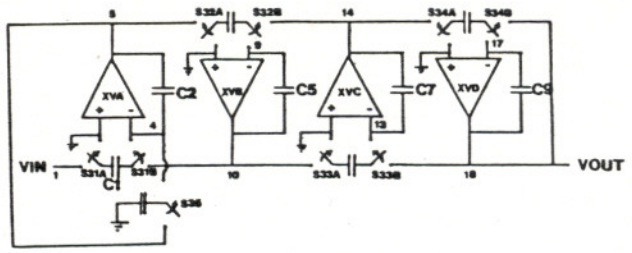
(a)



(b)

(c)

Fig. 7. Unit sample response of l-phase switched capacitor filter: (a) general network; (b) response to unit sample input in time slot i; (c) response, observed at time slot k. The dashed lines show the sample and hold effects.



(a)

INPUT DIANA

LDI

```
FOURTH ORDER BUTTERWORTH
.OPTIONS +APP -INT -TOP STORE NODE OPTS
.TRAN NOUT=300 DELTA=1
PRINT CL 1 5 10 13 18
INPUT CL V=T=0 0 4 0.5 2 4.51 2 1.5 0 1.51 0 2 CYC
INPUT DELTA V=T=0 0 1 1 0 2
XVDELTA 1 0 DELTA 0 1
C2 5 4 4.872
C5 9 10 11.76
C7 13 13 11.76
C9 17 18 4.872
XVA 5 0 0 4 1K
XVB 10 9 0 9 1K
XVC 14 2 0 13 1K
XVD 18 0 0 17 1K
S31A C1 1 0 CL 0 C=2 VT=1
S31B C1 10 4 CL 0 C=2 VT=1
S32A C5 2 9 CL 0 C=2 VT=1
S32B C5 9 14 CL 0 C=2 VT=1
S33A C5 10 0 CL 0 C=2 VT=1
S33B C6 18 13 CL 0 C=2 VT=1
S34A C9 0 14 CL 0 C=2 VT=1
S34B C9 17 18 CL 0 C=2 VT=1
S35 0 5 4 CL 0 C=1 VT=1
.END
```

DTI

```
S31A C1 1 0 CL 0 C=2 VT=1
S31B C1 10 4 CL 0 C=2 VT=1
S32A C5 9 0 CL 0 C=2 VT=1
S32B C5 14 9 CL 0 C=2 VT=1
S33A C6 10 0 CL 0 C=2 VT=1
S33B C6 18 13 CL 0 C=2 VT=1
S34A C8 14 0 CL 0 C=2 VT=1
S34B C8 18 17 CL 0 C=2 VT=1
S35 0 5 4 CL 0 C=1 VT=1
```

(b)

Fig. 8. (a) Fourth-order Butterworth filter and (b) DIANA input description for LDI and DTI.

frequency transforms of the unit sample responses at all time slots $k = 1 \cdots l$ followed by a FFT and the combination of these transforms, as described by (16). It also handles the sin $(x)/x$ effects, caused by the sample and hold effects [see dashed lines in Fig. 7(b) and (c)] either over a full or a partial period. Let us now look at two cases very often encountered in practice which are special cases of the discussed method and illustrate them by examples.

1) Filters with Input Sampled only During One Time Slot: A large number of switched capacitor filters published lately have the property that the input is only sampled during one particular time slot, say Δ_1. In this case all unit sample responses except one are zero and thus according to (16) only one unit sample simulation for Δ_1 is needed. Consider for example the case of the fourth-order Butterworth filter described by Jacobs *et al.* in [3] and shown in Fig. 8(a) together with the input code for simulations using the DIANA program in Fig. 8(b) (left).

It takes only 25 statements to describe the circuits topology and run control. Notice that 300 points of the unit sample response are requested with time step DELTA = 1 as discussed in Section II.

The switch models used here are capacitive double throw switches as described by the $S3$ model in Fig. 2. They are controlled by clock INPUT CL. As stated in [3], the frequency response depends strongly on the clocking phase: when clocked as in Fig. 8(a) the principle of the lossless digital integrator (LDI) is used. Inverting the clocks of switches $S32A$, $S32B$, $S34A$, and $S34B$ gives a direct transfer integrator (DTI) with larger delay. The underlined statements in Fig. 8(a) show the input changes in order to modify the phase of the above switches. Fig. 9(a) shows the unique unit-sample response computed by DIANA for the LDI (curve 1) and the DTI (curve 2) case. Fig. 9(b) shows the frequency response obtained from a FFT on Fig. 9(a) for both LDI and DTI.

These results agree fully with the measurements presented in [3]. This simulation takes 18 s CPU time on an IBM 370/158 which clearly shows the efficiency of the simulation method. The same example can easily be run on a minicomputer such as the PDP 11/40.

2) Filters Driven From a Sample and Hold Input: Some filters are driven from an input which is sampled in time slot i [time t_{i-1}, see Fig. 7(b)] and held over clock period T. The output is sampled, say, in time slot k (time t_{k-1}).

It is easy to see that in this case (16) has to be modified into

$$H'_k(j\omega) = e^{-j\omega(t_{k-1} - t_{i-1})} \left[e^{-j\omega T} \sum_{j=1}^{i-1} H_{k,j} + \sum_{j=i}^{l} H_{k,j} \right]. \tag{17}$$

The phase factor $\exp(-j\omega(t_{k-1} - t_{i-1}))$ results from delay between input and output samples whereas the terms in brackets account for responses due to the previous input sample, respectively, the actual input sample.

Notice from (17) that also in this case the response can be obtained from the FFT of the unit sample responses $h_{k,j}$ of the circuit.

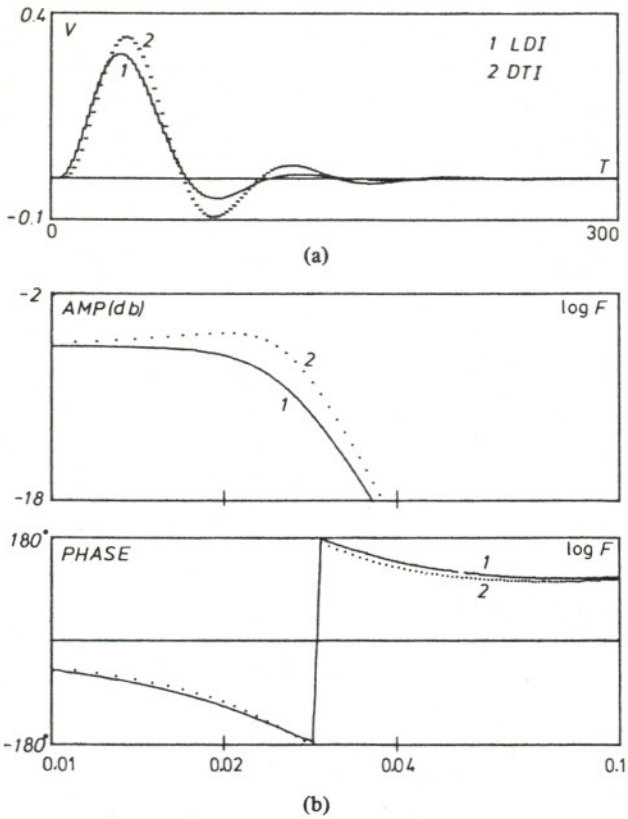


Fig. 9. (a) Impulse response for the circuit in Fig. 8(a) for LDI and DTI clocking. (b) Amplitude and phase responses resulting from FFT on Fig. 9(a). Notice that F is the frequency normalized to the sample frequency f_s, i.e., $F = f/f_s$.

Simulating the circuit in Fig. 6(a) while sampling input and output during Δ_2 and holding both constant over period T results in curve 3 in Fig. 6(b). This result can easily be verified starting from difference equations. Fig. 6 clearly demonstrates how careful one has to be in defining the transfer function of switched capacitor networks and indicates the usefulness of a simulation technique in this field.

B. Continuous Inputs

The above described method will not be correct, when the applied input is continuous. The difference will be especially important, when a continuous capacitive (or resistive) path exists between input and output. The importance of this effect, mainly a suppression of the effects of the sample and holds, which generate additional sin $(\omega T/2)/(\omega T/2)$ components in the frequency domain, has been demonstrated by Y. P. Tsividis [10]. The greatest difficulty, prohibiting normal simulation of the frequency response of circuits with a continuous I/O path, is caused by the fact that the output is a mixture of discrete and analog signals.

A technique will be demonstrated now, making it possible to simulate switched capacitor systems with continuous inputs and continuous I/O paths still using the unit sample responses $h_{k,i}(t)$ defined in Section IV-A.

Let us again use the example of Fig. 6(a) to illustrate the technique of which a rigorous proof is given in the Appendix.

Suppose $v_{in}(t)$ is a continuous sinusoidal input of amplitude 1. Due to the continuous coupling during Δ_2 by capacitor $2C$, the output is a mixture of sampled and continuous signals as is clear from Fig. 10(d) which shows a time domain simulation of the output using the DIANA program. As given, in general, in the Appendix the output can be considered as the superposition of three components shown for this particular case in Fig. 10(a)–(c) and which are:

1) the continuous input in each time slot $\Delta^{(k)}$ weighted by the "gain" defined by the instantaneous capacitive feedthrough through the capacitive I/O path in $\Delta^{(k)}$ [in this case zero during Δ_1 and $\frac{1}{2}$ during Δ_2, see Fig. 10(a)]. A different gain may exist for every time slot;

2) the inverted backward folded sample and hold version of the signal 1) as shown in Fig. 10(b). The result of adding 1) and 2) is the shaded area in Fig. 10(a);

3) in each time slot the sample and hold version of the output, due to a piecewise constant input, sampled at the *end* of the time slot [see Fig. 10(c)].

Notice now the following:

a) terms 1) and 2) disappear when no continuous I/O coupling is present such as in Fig. 8(a);

b) the frequency response in the baseband can still be obtained by using the FFT terms $H_{k,i}(e^{j\omega T})$ obtained from the unit sample responses $h_{k,i}(t)$ as discussed in Section IV-A. This is illustrated in Table III.

Indeed the baseband frequency component for time slot $\Delta^{(k)}$ in 1) is nothing else than the *first sample* of $h_{k,k}(t)$ or $h_{k,k}(0)$ weighted by duty cycle ρ_k since $h_{k,k}(0)$ represents the instantaneous feedthrough from input to output in $\Delta^{(k)}$.

Term 2) for $\Delta^{(k)}$ is the same as 1), but including sin $(x)/x$ effects for $\Delta^{(k)}$ and a forward shift of the input over $\rho_k T = \Delta^{(k)}$.

Term 3) results from the FFT's of all $h_{k,i}(t)$ $(k,i = 1 \cdots I)$ whereby however the appropriate phase factor is necessary to take into account the input sampling at the *end* of each time slot as well as duty cycle and sin $(x)/x$ effects (see Table III).

This algorithm is also implemented in the post processor of the DIANA program, and curve 1 on Fig. 6(b) shows the response of Fig. 6(a) to a continuous input as simulated by DIANA.

Notice the big difference with respect to a response to a S/H input (curve 3) due to the suppression of sample and hold effects in the continuous case by the capacitive I/O coupling.

The following two examples show practical existing filters with continuous coupling effects.

1) Simulation of a 60 Hz Notch Filter for PCM Filters: The above described method can also be applied to the notch filter of Fig. 11(a) [18] where the continuous I/O path is now resistive. A careful examination of Fig. 1(b) shows indeed that, if in an $\mathfrak{N}_{SC}$ circuit resistors are inserted into the matrix in their usual way, still a correct voltage solution is obtained provided the resistors are connected to dependent or independent voltage sources and virtual grounds. An enormous ratio of pole-zero frequency and sample frequency (60 Hz/128 kHz, which results in a ratio of 2133) can also be noted. The simulation over 3000 time points, together with the FFT over 16 000 points takes 2 min CPU time on an IBM 370/158. Amplitude and phase of the frequency response are shown in Fig. 11(b). This example shows clearly that also $\mathfrak{N}_{SC}$ networks with continuous resistive paths can be simulated.

2) Simulation of a Pole-Zero High-Pass Filter: Fig. 12(a) shows a simple pole-zero filter for audio treble tone control.

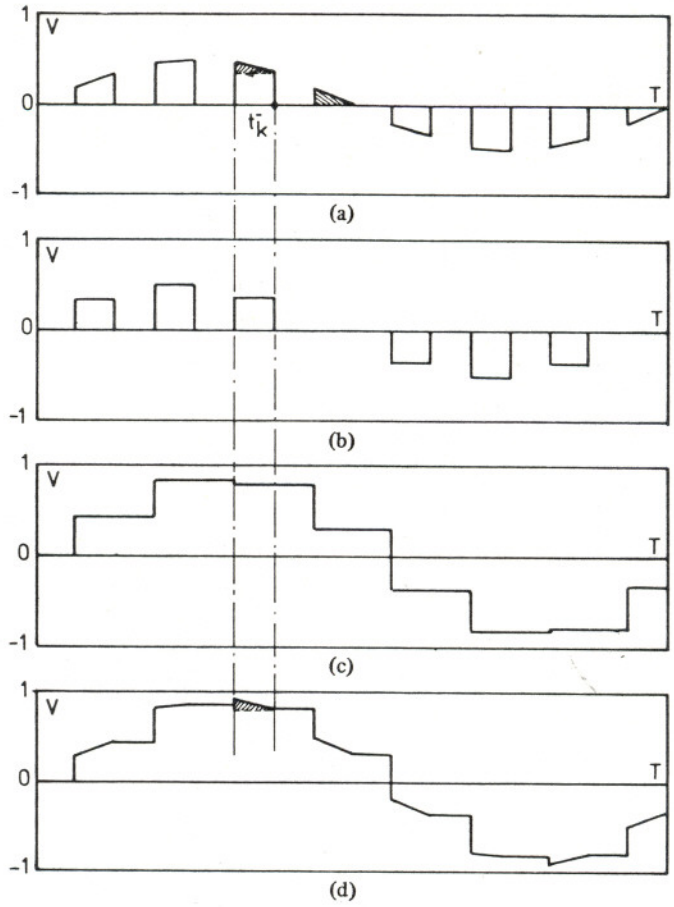


Fig. 10. Components of the time response of the passive low-pass filter of Fig. 6(a) for a sinusoidal input of unity amplitude.

TABLE III
BASEBAND FREQUENCY DOMAIN COMPONENTS CORRESPONDING TO TIME DOMAIN TERMS 1)–3) FOR A CONTINUOUS INPUT

$$f_k = \frac{\sin(\omega\rho_k T/2)}{\omega\rho_k T/2} e^{-j\omega\rho_k T/2}$$

$\sum_{k=1}^{l} \rho_k h_{k,k}(0)$	$- \sum_{k=1}^{l} \rho_k h_{k,k}(0) e^{j\omega\rho_k T} f_k$	$+ \sum_{k=1}^{l} \sum_{i=1}^{l} H_{k,i}(e^{j\omega T}) e^{j\omega(t_i - t_{k-1})} \rho_k f_k$
Terms 1)	Terms 2)	+ Terms 3)

Clearly there is a direct capacitive I/O path through C_1 and C_2. Fig. 12(b) shows three frequency responses computed by DIANA. The curves 1 and 2 are for a continuous input, but respectively for a duty cycle $\rho = 0.5$ [$C1$1 and $C1$2 in Fig. 12(a)] and $\rho = 0.25$ ($C1'$ and $C2'$). Curve 3 (dotted) is the response when the input is sampled and held over clock period T (notice sin $(x)/x$ effects). The case with $\rho = 0.25$ has been breadboarded and measured. The results are indicated by the dots in Fig. 12(b) showing good agreement with simulation.

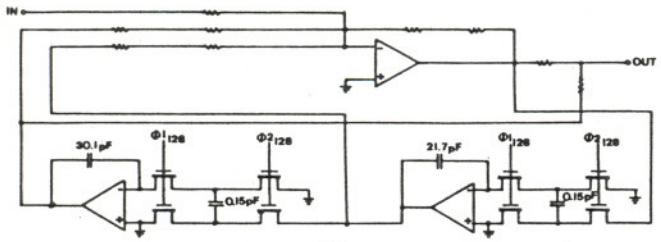
This practical example clearly demonstrates the influence of duty cycle and continuous coupling, and the usefulness of simulation for such cases.

V. Noise and Sensitivity Calculations [20]

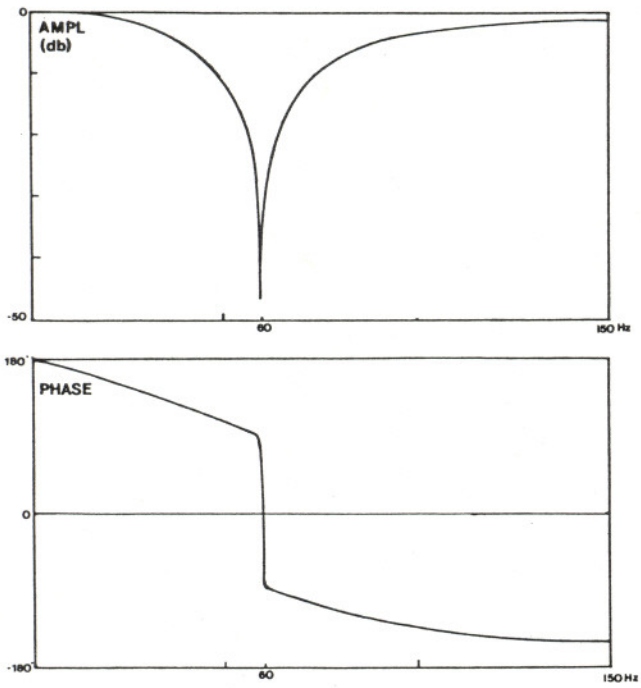
It can be proven [20] that an adjoint network for switched capacitor networks can be defined. The interreciprocal network can be formed, changing voltage sources in "charge souces" and using charge-pulses as circuit excitation. The adjoint network has the interesting property that the transfer function in the frequency domain, looking at one clock-phase on the output, can be obtained doing only one simulation in the time-domain instead of N as was stated before. This leads to interesting consequences. Using the adjoint network, noise and sensitivity calculations are simplified as will be demonstrated in a later paper.

VI. Conclusions

In this contribution, a simple, but very general method is presented for the simulation of switched capacitor networks with arbitrary clocking sequences, based on MNA with an appropriate switch model. This method is directly compatible with algorithms used in existing circuit simulation programs.



(a)



(b)

Fig. 11. Simulation of the frequency response of a 60 Hz notch filter with continuous resistive I/O coupling.

Time as well as frequency amplitude and phase simulation is possible even with continuous I/O coupling. Top-down design is possible. Complete A/D-D/A convertors and full MOS-LSI switched capacitor filters can be simulated on a 64 kbyte minicomputer; fully mixed analog–digital LSI structures can be simulated on larger computer systems.

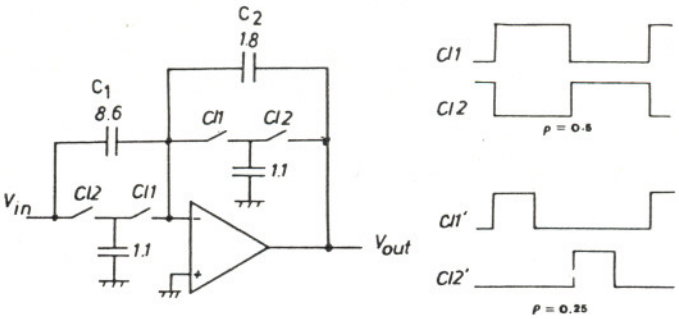
Appendix
On the Evaluation of Switched Capacitor Circuits with Continuous Input and Capacitive I/O Path

Let T be the period of the clock sequence and t_{k-1}, t_k, t, and time slot $\Delta^{(k)}$ defined as in Fig. 1(a). Starting from the continuous MNA equation (5), after eliminating $q^{(k)}(t)$ and solving for the node voltage vector $v^{(k)}(t)$ one obtains

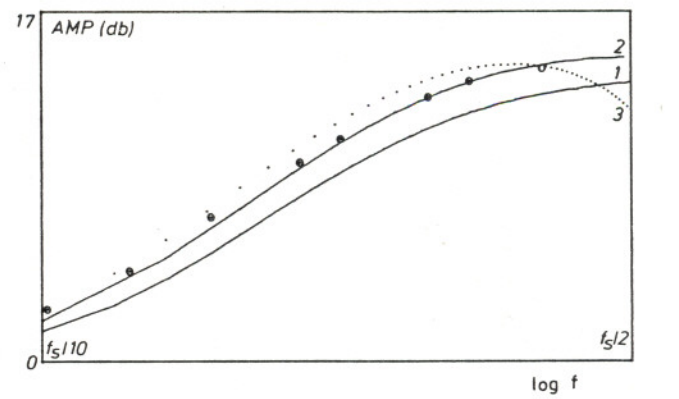
$$v^{(k)}(t) = \alpha^{(k)} v_{in}(t) \cdot p^{(k)}(t) + \beta^{(k)} v^{(k-1)}(t_{k-1}^-) p^{(k)}(t) \quad \text{(A1)}$$

where $v_{in}(t)$ is the vector of input voltages, $v^{(k)}(t)$ is the node voltage vector in time slot $\Delta^{(k)}$, and $p^{(k)}(t)$ is a window function:

$$\begin{cases} p^{(k)}(t) = 1 & \text{for } t_{k-1} + nT \leqslant t_k \leqslant t_k + nT \\ p^{(k)}(t) = 0 & \text{otherwise.} \end{cases}$$



(a)



(b)

Fig. 12. Simulation of a pole-zero filter with capacitive I/O coupling: Curve 1–with clocks $Cl1$ and $Cl2$ and continuous input; Curve 2–with clocks $Cl1'$ and $Cl2'$ and continuous input; Curve 3–with sample and hold on the input over period T; ⊙–measurements on breadboard using clocks $Cl1'$ and $Cl2'$.

Multiplication with $p^{(k)}(t)$ is an operation making it possible to handle the time slots separately and making Fourier-transform of the result possible. For example $v^{(k)}(t) = v(t)p^{(k)}(t)$ is the node voltage vector during interval k. On the other hand at the *instant* t_k^- at the end of $\Delta^{(k)}$ (A1) reads

$$v^{(k)}(t_k^-) = \alpha^{(k)} v_{in}(t_k^-) + \beta^{(k)} v^{(k-1)}(t_{k-1}^-). \quad \text{(A2)}$$

Multiplication of (A2) with $p^{(k)}(t)$ represents a backward folded sample and hold version of $v^{(k)}(t_k^-)$ [see Fig. 10(b) and (c)], i.e.,

$$v^{(k)}(t_k^-) \cdot p_k(t) = \alpha^{(k)} v_{in}(t_k^-) \cdot p^{(k)}(t) + \beta^{(k)} v^{(k-1)}(t_{k-1}^-) \cdot p^{(k)}(t). \quad \text{(A3)}$$

Subtracting (A3) from (A1) gives

$$v^{(k)}(t) = \alpha^{(k)} v_{in}(t) \cdot p^{(k)}(t) - \alpha^{(k)} v_{in}(t_k^-) p^{(k)}(t) + v^{(k)}(t_k^-) p^{(k)}(t). \quad \text{(A4)}$$

A careful consideration of (A4) shows that within time slot $\Delta^{(k)}$ the node voltage vector $v^{(k)}(t)$ is the superposition of terms 1)–3) which are the ones mentioned in Section IV-B.

Indeed from (A3) it follows that $\alpha^{(k)}$ is the direct capacitive feedthrough since the memory effects are represented by $\beta^{(k)}$ and thus terms 1) and 2) have their meaning explained in Section IV-B.

Term 3), as is clear from (A3) is the response of the circuit for a piecewise constant input sampled at the *end* of $\Delta^{(k)}$ (i.e., t_k^-), but shifted backwards to the beginning of $\Delta^{(k)}(t_{k-1}^+)$ and

then held constant over $\Delta^{(k)}$ due to the $p^{(k)}(t)$ term. This proves the method illustrated in Section IV-B.

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